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DESIGN AND IMPLEMENTATION OF POWER FACTOR CORRECTION (PFC) CONVERTER WITH AVERAGE CURRENT MODE CONTROL USING DSP

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Abstract- This paper presents a digital controlling method for power factor correction converter with boost structure, by applying average current controlling operation at a fixed frequency, to be used at 90-265 V_{rms} line voltage, based on being applied on DSP. This method which is based designing in analogue domain and converting the resulting model in to digital domain will be discussed in this paper. The obtained results of applying this method on practical circuit, with power of 1200w, which shows a power factor more than 0.99, are also provided in this article.

Keywords: Average Current Mode, Power Factor Correction, Boost Converter, DSP.

I. INTRODUCTION

Digital signal processing (DSP) are designed for the purpose of control loop implementation, and are widely used on motor controlling, uninterruptible power supplies (UPS) and movement controlling applications. Owing to their high CPU bandwidth and the peripherals, integrated with them, in order to be used in power electronics, such as analogue to digital converter, pulse width modulation and power stage protection, low cost and high efficiency, which have caused the designers to take DSPs as a suitable option for control and power conversion applications. Comparing to the conventional controlling methods in analogue domain, DSP controllers have the following advantages : low level of sensitivity versus environmental changes and aging , high resistance for noise, easy application of developed controlling algorithms , high flexibility in case of alternating the model, in order to response to consumes requirements. However, use of DSPs in power supply applications being the analogue designer into new challenges in attempt of converting the existing analogue region into a new digital one. Many dependent factors in designing and implementing a digital control loop, for controlled DSP power supplies need to be considered.

For the analogue designer be able to convert the controlling analogue hardware to its opposite point, the digital software, it's necessary for the designer to design analogue control blocks and dependent parameters in digital region. Diverse dimension of implementing the controlling circuit by using a DSP, based on the average current mode control of power factor correction, is discussed in this paper. Differences between the control loop parameters in analogue region are designed before being converted to digital region.

The required scaling and normalization will described in the practical input interval (85-265 VAC, 47-63 Hz), in case of implementing based on a 16-bit and fixed point DSP (TMS320F2808). First the control loop is considered and then required current and voltage loop compensations are generated, next these compensations are converted into digital domain, and finally their implementation is presented as software [1, 2].

II. PFC STAGE DIGITAL CONTROLLER DESIGN

Figure 1 shows a PFC control loop, which is controlled by DSP. In this figure, those circuits which measure current and voltage and change them into suitable samples, are replaced by block with adequate gain. These blocks are shown as K_f, K_s and K_d. The multiplier gain, K_m, is also added to the control block. K_m allows the reference signal, I_{ref}, to be adjusted depending on the operational interval of the converter input voltage. The inner loop, which is a current loop, is programmed by the reference current, I_{ref}. The current loop's input in the power stage is the pulse width ratio command, d, and its output is the inductor current, I_{in}. The G_{ca} current controller, which provides a desirable output for U_{ca}, is designed in a way that the inductor current I_{in}, tracks the reference current I_{ref}. The output voltage loop is programmed according to the reference voltage, V_{ref}. The voltage loop's input in the power section, is the U_{nv}, (voltage controller output), and its output the DC voltage called V_o. The G_{vea} voltage controller, which provides a suitable U_{nv} to controller the amplitude of the reference current, I_{ref}, is designed in a way that for any taken line voltage and applied load current, the V_o is remained at the reference level. In order to implement this controlling method, calculating the current and voltage controllers is necessary.

Respectfully, determining the blocks shown in Figure 1 is also required. Specially, this method will be implemented by software using a TMS320F2808 controller which works by the fixed point method.

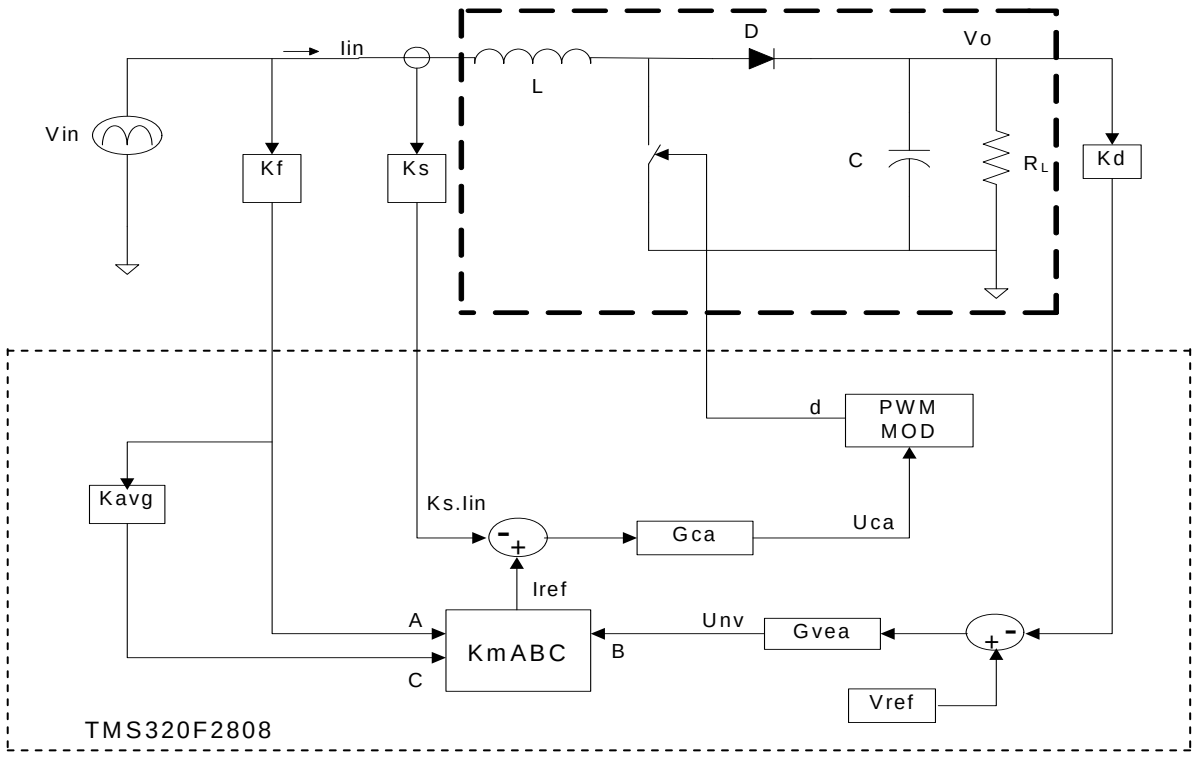

Figure 1. Control loop block diagram of the DSP controlled PFC stage [2]

III. CURRENT AND VOLTAGE LOOP COMPENSATOR

High frequency approximation of the current loop of the power stage is as following [1]:

$$G_{id} = \frac{\hat{I}_{in}}{\hat{d}} = \frac{V_o}{SL} \tag{1}$$

The loop gain for the current loop is derived from PFC block diagram shown in Figure 1:

$$T_i = G_{id}\, K_S\, G_{ca}\, F_m \tag{2}$$

Therefore the modulator gain will be following:

$$F_m = \frac{\hat{d}}{\hat{U}_{ca}} \tag{3}$$

A part of this modulation is performed by software and the other part is performed by PWM DSP hardware. The software uses the modulator input or in other words the current controllers input (U_{ca}) and calculates the pulse width for the PWM hardware in TMS320F2808 , and the PWM hardware uses the calculated pulse width to generate a convenient PWM signal for the PFC switch. The software is implemented in such a way that when the modulator input, U_{ca}, is 1, the modulator output or in other words the pulse width to switching period ratio, have to be 100%. This means, that the modulator gain in this case is F_m=1.

So, the required current error compensating amplifier, for a current loop with f_{ci} as the crossover frequency will be as following:

$$G_{ca} = \frac{2\pi f_{ci} L}{K_S V_o} \tag{4}$$

After the current loop is closed, the transfer function for the power stage of the voltage loop can be calculated using the following equation [2]:

$$G_{vc} = \frac{\hat{V}_o}{\hat{U}_{nv}} = \frac{K_m}{2 K_f K_S}\left[\frac{V_{\min}}{V_{\max}}\right]^2 \frac{Z_f}{V_o} \tag{5}$$

where Z_f represents the equivalent impedance of the parallel branch containing the line capacitor and loop impedance, and is calculated as shown below [2]:

$$Z_f = \frac{Z_o}{1 + SCZ_o} \tag{6}$$

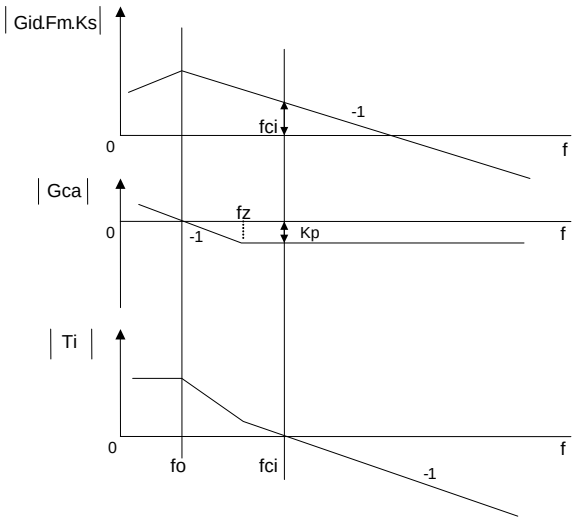

Figure 2. Bode plot for current loop compensation [2]

For a constant power load of P_o, load impedance Z_o is:

$$Z_o = \frac{-V_o^2}{P_o} \tag{7}$$

Using the block diagram shown in Figure 1, the loop gain in the voltage loop will be calculated as:

$$T_v = K_d\, G_{VEA}\, G_{vc} \tag{8}$$

The required voltage error amplifier compensator, for voltage loop crossover frequency, can be calculated using the loop gain equation [2, 5]:

$$G_{VEA} = \frac{2 K_f\, K_S}{K_d\, K_m}\left[\frac{V_{\max}}{V_{\min}}\right]^2 \left.\frac{V_o}{Z_f}\right|_{f=f_{cv}} \tag{9}$$

IV. SOFTWARE IMPLEMENTATION OF CURRENT AND VOLTAGE LOOP COMPENSATOR

The current and voltage loop controllers , discussed at the previous section , before being implemented by software using TMS320F2808, have to be converted to digital form, For instance the current controller can be written as following:

$$G_{ca}(S) = K_p \frac{1 + T_I S}{T_I S} = K_p + \frac{K_I}{S} = \frac{U_{ca}}{E(S)} \tag{10}$$

where K_p is current compensator amplitude which was considered in the previous section, and E is the current error signal. The zero $W_L = 2\pi f_z = 1/T_I$ of the compensator, is usually chosen somewhere below the crossover frequency, f_{ci}, in order to maintain adequate phase margin. A graphical design of the loop compensator by bode diagram, is shown in Figure 2. The first diagram in Figure 2 shows the gain diagram for all of the control blocks in the current loop, or in other words, the G_{id}, F_m and K_s, except the current compensator G_{ca}. Gain diagram for G_{ca} compensator is shown in the second diagram of Figure 2 which is derived in order to reach the, T_I, the designed loop gain, shown in the bottom of Figure 2. As it's obvious from Figure 2 the power stage has a-1 slope. The compensator zero f_z is chosen in a way that in a designed crossover frequency of f_{ci}, the phase margin would be 45°. However, in digital implementation some of this phase margin can be lost because of control loop sampling and computation delay. In order to compensate this loss, it's necessary to choose the compensator's zero somewhere a little more below the crossover frequency, as shown in Figure 2.

In discrete form, the mentioned current controller, can be expressed as below:

$$U_{ca}(n) = K_p\, E(n) + K_I\, T_S \sum_{j=0}^{n} E(j) \tag{11}$$

where T_s is the loop sampling time. This controller is implemented by integral component correction and output saturation, as shown below:

$$U_{ca}(n) = K_o E(n) + I(n) \tag{12}$$

$$I(n) = I(n-1) + K_1 E(n) + K_{corr} E_{pi} \tag{13}$$

$$E_{pi} = Us - U_{ca}(n) \tag{14}$$

where

$$U_S = U_{ca,\max} \quad \text{when} \quad U_{ca}(n) \geq U_{ca,\max}$$

$$U_S = U_{ca,\min} \quad \text{when} \quad U_{ca}(n) \leq U_{ca,\min}$$

Here U_S shows the final output of the current controller with output saturation and integral component correction. The coefficients of the above equation are designed as following:

$$K_0 = K_p\,, \quad K_1 = K_I\, T_S\,, \quad K_{corr} = \frac{K_1}{K_0}$$

This equation can be easily implemented by software using TMS320F2808.

V. PFC STAGE DIGITAL CONTROLLER DESIGN EXAMPLE

Using the proposed method in this paper a PFC converter with the following characteristics have been designed and implemented: L_{Boost}=1 mH, C_o=2 mF, 220 VAC input, 400 VDC output, 50 Hz input frequency, 1200 W output power, 50 kHz switching frequency, f_{cv}=10Hz voltage loop bandwidth and f_{ci}=8kHz current loop band width .In order to provide the maximum output power, using a minimum value of input voltage, the maximum input current should be:

$$I_{\max} = \frac{2\, P_o}{V_{\min}} = 15 \text{ A}$$

Various parameters related to the gain are calculated as below:

$$K_f = \frac{1}{410}\,, \quad K_d = \frac{1}{410}$$

$$K_s = \frac{1}{15}, \quad K_m = \frac{410}{109.95} = 3.7268$$

Considering f_{ci}=8 kHz, the current controller amplitude would be $|G_A|$ = 1.884.

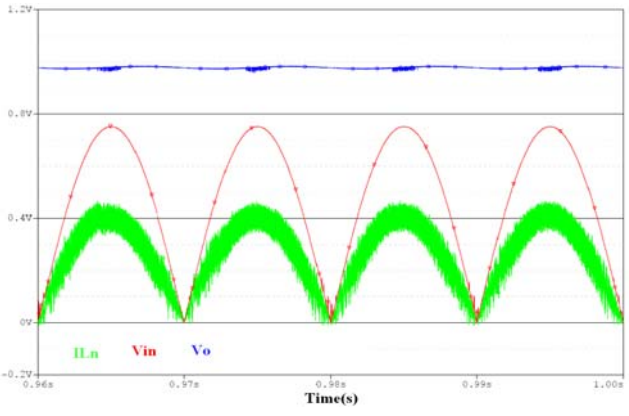

Figure 3. Simulation results of the input and output waveforms

The zero of the PI compensator will be located on 4 kHz. Therefore the total time constant for the current compensator equals:

$$T_{IC} = \frac{1}{2\pi \times 4000} = 39.79 * 10^{-6}$$

So the current loop controller will be as following:

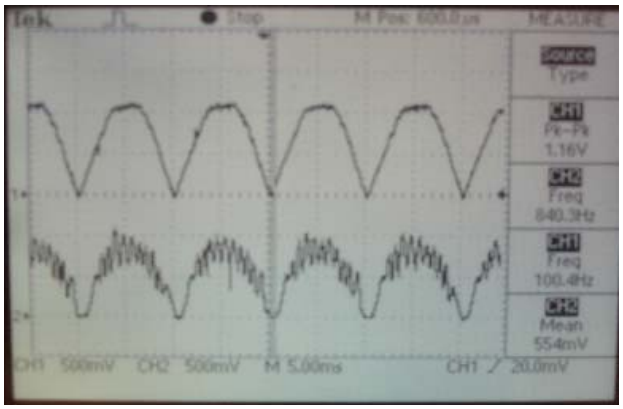

Figure 4. Experimental results of the input voltage and inductor current (above waveform for input voltage and other waveform for current)

$$G_{ca} = 1.332\frac{1+(39.79*10^{-6})S}{(39.79*10^{-6})S}$$

$$G_{ca} = K_{pi} + \frac{K_{Ii}}{S} = \frac{U_i(S)}{E_i(S)}$$

where

$$K_{Ii} = 33.48*10^3, \qquad K_{pi} = 1.332$$

Considering f_{cv}=10 Hz, the voltage controller amplitude would be $|G_{VEA}|$ = 8.57. The zero of the PI voltage loop compensator will be located on 10 Hz. Therefore the total time constant equals:

$$T_{IV} = \frac{1}{2\pi\times 10} = 15.9155*10^{-3}$$

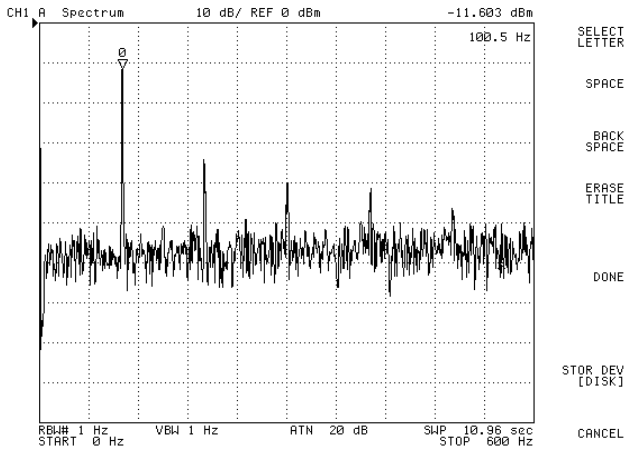

Figure 5. Frequency spectrum of inductor current for PFC stage (measured by a spectrum analyzer)

So the voltage loop controller will be as following:

$$G_{VEA}(S) = 6.06\frac{1+(15.9155*10^{-3})S}{(15.9155*10^{-3})S}$$

$$G_{VEA}(S) = K_{pv} + \frac{K_{IV}}{S} = \frac{U_v(S)}{E_v(S)}$$

where

$$K_{IV} = 380.6, \qquad K_{pv} = 6.06$$

VI. SIMULATION AND EXPERIMENTAL RESULTS

In order to validate the presented study, simulation and experimental results for the converter are shown in Figure 3 and Figure 4.The simulation results based on OrCad are shown in Figure 3. The parameters used in the simulation are mentioned in previous section. When the output current is full load, the input current and voltage waveforms are shown in Figure 3.

Figure 4 shows the input voltage and current which are measured using a digital oscilloscope. Note that the scaling has been chosen in a way that both of the waveforms can be compared and measured. Figure 5 also shows the frequency spectrum of the input current, which is measured by a spectrum analyzer. The measurements are proof for the power factor of more than 0.99. THD of the input current is 9%.

VII. CONCLUSIONS

PFC convertors are the best choice for digital controlling, because they need control loops with lower band width. Specially, in BOOST PFC converters, using the current average control, the current loop bandwidth is somehow below 5 kHz.

However the voltage loop bandwidth is also below 100Hz.Comparing to the analogue control circuit, digital control designing based on DSP, allows a more sufficient implementation of the circuit for a wide range of inputs also, by this method, one can be able of applying the required limitations on the current harmonics based on European Standard EN61000-3-2 and Japanese standards.

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BIOGRAPHY

Hamid Jangi Bahador was born in Tabriz, Iran, 1981. He received the B.Sc. degrees from Iran University of Science and Technology, in 2000, the M.Sc. degrees from Sharif University of Technology in Tehran, Iran, 2008, all in electrical engineering. Since 2008, he has been an academic member of Seraj Higher Education Institute, Tabriz, Iran.