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DSTATCOM BASED FIVE-LEVEL CASCADE H-BRIDGE MULTILEVEL INVERTER FOR POWER QUALITY IMPROVEMENT

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Abstract- Power electronic device, nonlinear and unbalanced loads have given rise to power quality problem in distribution systems. Due to factors like competitive generation patterns in a deregulated electric grid and an increasing level of sensitive end user devices, it has become necessary to ensure both reliable and power quality to the end customer. One way to betterment the power quality is using a Distribution Static Compensator (DSTATCOM) to compensate active and reactive power, power factor correction and voltage stability. In this paper, the design of a DSTATCOM employing a Cascade H-Bridge Multilevel Inverter (CHBMLI) in a medium voltage distribution power system is presented. The phase shifted PWM technique is used to generate firing angles to CHB inverter switches. In this study, the proposed controller in DSTATCOM structure in order to power quality improvement based proportional integral (PI) controllers and p-q coordinates. Simulation result prepared by the help of Matlab/Simulink software. The Simulink results will be presented to verify the performance of the proposed multilevel DSTATCOM.

Keywords: DSTATCOM, Cascade H-Bridge, Phase Shift PWM Modulation.

I. INTRODUCTION

The problems which affect the power quality in distribution systems are pertaining to the specifications of the loads. Some of the most popular effects are: the harmonics generated by nonlinear loads and unbalanced loads and the low-power factor of the loads [1]. A part from nonlinear loads, events like motor starting, capacitor switching and unusual faults could also impose power quality (PQ) problems. Fixed, mechanical switched reactor/capacitor banks and Static VAR Compensator (SVC) have been employed in power industry for improvement of system performances [2].

These types of compensation have some disadvantages such as limited bandwidth, slower response, more losses and big size. Recently, due to fast extension of high power switching elements such as IGBTs and IGCTs, DSTATCOM is a shunt custom power devices, has been recognized the second generation compensator for power factor correction, load balancing, voltage regulation and harmonic filtering in distribution systems [3].

In this paper, a five-level cascade H-bridge inverter based DSTATCOM configuration has been presented. The adoption of cascade H-bridge inverter for DSTATCOM applications causes to decrease the device voltage and the output harmonics by increasing the number of output voltage levels. Inverter circuit is heart of DSTATCOM and various inverter topologies can be utilized in applications of DSTATCOM such as: cascaded h-bridge, neutral point clamped (NPC) and flying capacitor (FC) [4]. In particular, among these topologies, CHB inverters are being widely used because of their modularity and simplicity. Various modulation methods can be applied to CHB inverters. There are various modulation methods, but phase shift modulation has used in this paper. CHB inverters can also increase the number of output voltage levels easily by increasing the number of H-bridges cells [5]. This paper presents a DSTATCOM with a PI controller based five-level CHB multilevel inverter for the current harmonic, voltage flicker and reactive power mitigation of the nonlinear load.

II. CASCADE H-BRIDGE MULTILEVEL INVERTER

A three-phase structure of a five-level cascaded inverter is illustrated in Figure 1. The multilevel inverter using cascaded-inverter with separate dc sources (SDCSs) synthesize a favorable voltage from several independent sources of dc voltages, which may be achieved from batteries, solar cells and fuel cells [6]. This structure recently has become very widespread in ac power supply and adjustable speed drive applications.

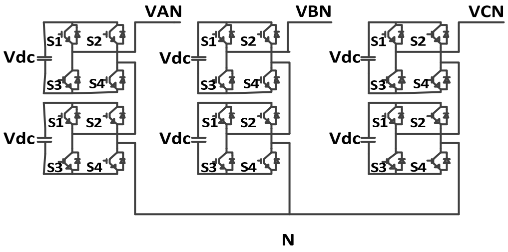


Figure 1. Five level cascade H-bridge inverter structure

The output of each cell will have three levels $+V_{dc}$, 0 and $-V_{dc}$ that obtained by connecting the dc source to the ac output by different combinations of the four switches S_1, S_2, S_3 and S_4. To obtain $+V_{dc}$, switches S_1 and S_4 are turned on, whereas $-V_{dc}$ can be obtained by turning on switches S_2 and S_4. By turning on S_1 and S_2 or S_3 and S_4, the output voltage is 0. The output voltage is the sum of the voltage that is generated by each cell. The numbers of output voltage levels are $2(m+1)$ where m is the number of cells. The output voltage of a cascaded H-bridge inverter leg is obtained by adding the single H-bridge output voltages as follows [7]:

$$V_o(t) = \sum_{k=1}^{n} v_{o_k}(t) \tag{1}$$

where k is number of kth cell. The voltage level and switching state of the five-level CHB inverter are shown in the Table 1. Table 2 shows the component requirements for m-level cascade H-bridge inverter for a three-phase setup.

Table 1. Switching state for five level cascade H-bridge inverter

Switching State								
S_1	S_2	S_3	S_4	S'_1	S'_2	S'_3	S'_4	V_{ao}
1	0	1	0	0	1	0	1	$2V_{dc}$
1	1	1	0	0	0	0	1	V_{dc}
1	0	0	0	0	1	1	1	V_{dc}
1	0	1	1	0	1	0	0	V_{dc}
0	0	1	0	1	1	0	1	V_{dc}
1	1	1	1	0	0	0	0	0
1	1	0	0	0	0	1	1	0
1	0	0	1	0	1	1	0	0
0	1	1	0	1	0	0	1	0
0	0	1	1	1	1	0	0	0
0	0	0	0	1	1	1	1	0
0	1	1	1	1	0	0	0	$-V_{dc}$
0	0	0	1	1	1	1	0	$-V_{dc}$
0	1	0	0	1	0	1	1	$-V_{dc}$
1	1	0	1	0	0	1	0	$-V_{dc}$
0	1	0	1	1	0	1	0	$-2V_{dc}$

Table 2. Component requirements for m-level cascade h-bridge inverter

m-Level Cascade H-Bridge	Number of elements
DC bus capacitors	3(*m*-1)/2
Main diodes	6(*m*-1)
Main switches	6(*m*-1)
Clamping diodes	0
Clamping capacitors	0

Figure 2 shows an example phase voltage waveform for a five-level cascaded H-bridge inverter with four dc source. The main advantages and disadvantages of the cascade H-bridge multilevel inverter are as follows [8]:

Advantages:

- Requires a low number of components per level.
- Possibility to implement soft-switching.
- Uncomplicated voltage balancing modulation.
- Modularized structure without clamping component.

Disadvantages:

- Needs separate isolated dc sources for real power transfer.
- No common DC-bus.

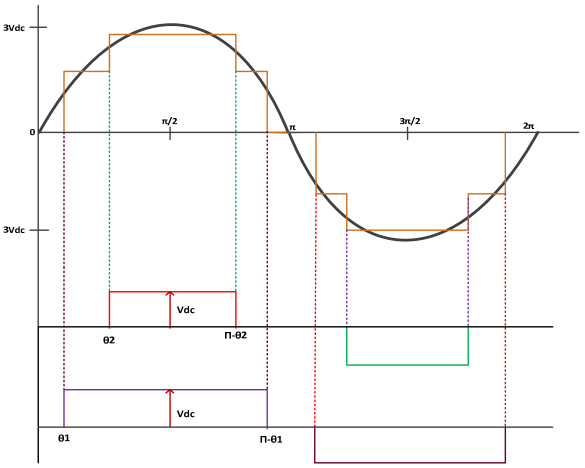


Figure 2. Output voltage waveform for five level cascade H-bridge inverter

III. MODULATION STRATEGY

The modulation schemes for the multilevel CHB inverters can be generally assortment into carrier based modulation, space vector modulation and staircase modulation with selective harmonic elimination [9]. The carrier-based modulation schemes for multilevel inverters are classified to phase-shifted and level-shifted modulations. In this paper, the inverter switches are controlled by pulse width modulation strategy employing phase shifted carriers (PSPWM).

Multilevel inverter with m voltage levels needs $m-1$ triangular carriers. In the phase-shifted multicarrier modulation, all the triangular carriers have the equal frequency and the peak-peak amplitude with the phase shift between any two adjacent carrier waves given by:

$$\varphi_{cr} = \frac{360^\circ}{m-1} \tag{2}$$

The frequency modulation index m_f is given by:

$$m_f = f_{cr} / f_m \tag{3}$$

where f_{cr} and f_m respectively mention to carrier signal frequency and fundamental signal frequency. The frequency of prevalent harmonic in the inverter output voltage is given by [10]:

$$f_{sw,inv} = (m-1) \times f_{sw,dev} \tag{4}$$

where $f_{sw,dev}$ represents the device switching frequency.

The modulated signal $V_{control}$ is compared with a phase shifted triangular signals in order to generate the switching signals. Figure 3 shows waveforms of carrier, modulating and command signals using phase shifted PWM method. The main parameters of the phase shifted PWM scheme are the amplitude modulation index of signal, and the frequency modulation index of the triangular signal [11]. In multilevel inverters, the amplitude modulation index m_a defined as:

$$m_a = V_{control} / V_{tri} \tag{5}$$

where $V_{control}$ is the peak amplitude of the control signal and V_{tri} is the peak amplitude of the triangular signals.

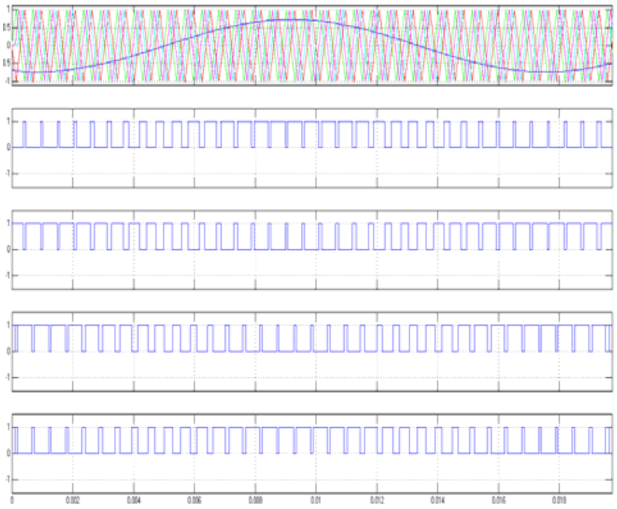


Figure 3. Phase shift PWM modulation and pulses for on phase

IV. REVIEW OF DSTATCOM

A. Operation of DSTATCOM

The DSTATCOM is a voltage or current source inverter based custom power device connected in shunt with the power system. It is connected near the load at the distribution systems [12, 19]. The basic structure of DSTATCOM is presented in Figure 4. As shown in Figure 4, DSTATCOM consists of an inverter, dc link capacitance C that providing the dc voltage for inverter, coupling inductance L used for current filter and reactive power exchange between DSTATCOM and power system and a control unit to generate PWM signals for the switches of inverter. In Figure 4, R_{dc} and R respectively represents switching losses in inverter and winding resistance of coupling inductance [13].

Exchange of reactive power between distribution system and DSTATCOM is achieved by regulating amplitude of the inverter output voltage V_i. The DSTATCOM operation is illustrated by the phasor diagrams shown in Figure 5.

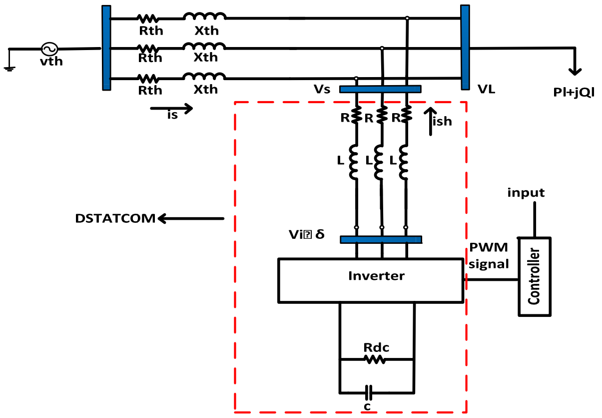
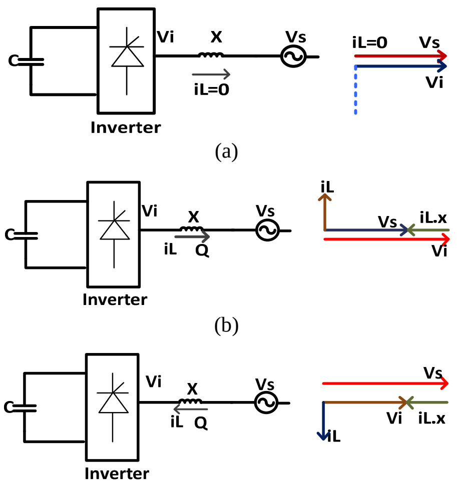


Figure 4. Basic structure of DSTATCOM in distribution system

If output voltage of DSTATCOM V_i is equal to AC system voltage V_s, exchange reactive power between DSTATCOM and gird will be zero and DSTATCOM operates in standby mode (Figure 5(a)).

If output voltage of DSTATCOM V_i is greater than ac system voltage V_s, DSTATCOM generate a capacitive reactive power (Figure 5(b)) and finally If output voltage of DSTATCOM V_i is lower than ac system voltage V_s, DSTATCOM absorbed an inductive reactive power (Figure 5(c)) [14].



(a)

(b)

(c)

Figure 5. Phasor diagrams for operation modes of DSTATCOM

Reactive and active power that generated or (absorbed) by DSTATCOM respectively is given by Equation (6) and Equation (7) [15].

$$Q = \frac{V_s}{X}(V_s - V_i \cos\delta) \tag{6}$$

$$P = \frac{V_s V_i}{X}\sin\delta \tag{7}$$

where X is reactance of coupling inductance and δ is phase angel between fundamental voltage of DSTATCOM and AC grid.

B. Five-Level Cascade H-Bridge Inverter Based DSTATCOM

In this study, five-level cascade h-bridge inverter is presented for power circuit of DSTATCOM. Power circuit of DSTATCOM based five-level cascade H-bridge inverter is illustrated in Figure 6.

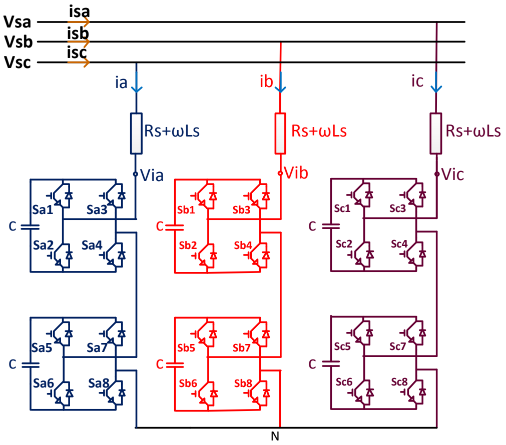


Figure 6. DSTATCOM five level cascade H-bridge inverter

D-STATCOM consists of six h-bridge cells, six dc-link capacitors C that providing the dc voltages to H-bridge cells and a coupling inductance with internal resistance $\omega L_s + R_s$ connecting to AC grid the inverter. From Figure 6, AC circuit equations of DSTATCOM in the stationary reference frame can be acquired as follows [16, 20]:

$$L_s \frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + R_s \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} - \begin{bmatrix} V_{ia} \\ V_{ib} \\ V_{ic} \end{bmatrix} \tag{8}$$

$$\vec{V_s} = \begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} \text{ and } \vec{V_i} = \begin{bmatrix} V_{ia} \\ V_{ib} \\ V_{ic} \end{bmatrix} \tag{9}$$

The $\vec{V_s}$ and $\vec{V_i}$ respectively are defined as complex voltage vector of network and complex voltage vector of inverter. Space vector theory based on synchronous reference frame is exerted to DSTATCOM. Coordination of space vector is shown in Figure 7. Stationary reference and synchronous rotating frame are respectively shown with $\alpha\beta$ and dq-axes.

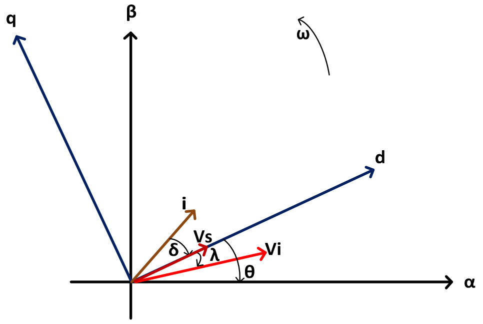


Figure 7. Coordinate system for synchronous rotating reference frame

Current vector and voltage vectors in complex plane are representing in stationary reference frame as follows [17]:

$$\vec{V_i} = V_{ia} + V_{ib}\,e^{j\varphi} + V_{ic}\,e^{j2\varphi} = V_i\,e^{j(\theta-\lambda)} \tag{10}$$

$$\vec{V_s} = V_{sa} + V_{sb}e^{j\varphi} + V_{sc}e^{j2\varphi} = V_s\,e^{j(\theta)} \tag{11}$$

$$i = i_a + i_b\,e^{j\varphi} + i_c\,e^{j2\varphi} = i\,e^{j(\delta+\theta)} \tag{12}$$

where $\varphi = 2\pi/3$, $V_{s(a,b,c)}$ and $V_{i(a,b,c)}$ respectively are instantaneous phase voltages of power system and DSTATCOM. The d-axis of the space vector figure and V_i are assigned together. By multiplying complex vectors in the stationary reference frame with unity space vector $e^{-i\theta}$ can transformed them into synchronous rotating as follows [16]:

$$L_s\,e^{-j\theta}\frac{d}{dt}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + R_s\,e^{-j\theta}\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} V_{sa} \\ V_{sb} \\ Vsc \end{bmatrix} e^{-j\theta} - \begin{bmatrix} V_{ia} \\ V_{ib} \\ V_{ic} \end{bmatrix} e^{-j\theta} \tag{13}$$

$$\begin{bmatrix} V_{sa} \\ V_{sb} \\ V_{sc} \end{bmatrix} e^{-j\theta} = v_{sd} + jv_{sq} \tag{14}$$

$$\begin{bmatrix} V_{ia} \\ V_{ib} \\ V_{ic} \end{bmatrix} e^{-j\theta} = v_{id} + jv_{iq} = v_i \cos\lambda - jv_i \sin\lambda \tag{15}$$

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} e^{-j\theta} = i_d + ji_q \tag{16}$$

By substituting (13), (14), (15) into (16), the circuit equations in dq-axis are achieved as (17) and (18) [16].

$$L_s \frac{di_d}{dt} + R_s i_d = v_{sd} - v_i \cos\lambda + L_s \omega i_q \tag{17}$$

$$L_s \frac{di_q}{dt} + R_s i_q = v_{sq} - v_i \sin\lambda - L_s \omega i_d \tag{18}$$

where, ω is frequency of power system. Maximum magnitude of inverter output voltage is expressed as [17]:

$$V = M_a V_{dc} \tag{19}$$

where M_a modulation is index and V_{dc} is dc-link voltage.

From instantaneous power quality on the DC and AC side of the inverter, power equation can be written as:

$$P_c = V_{dc} I_{dc} = \frac{3}{2}(v_{id} i_d + v_{iq} i_q) \tag{20}$$

where I_{dc} is the capacitor current.

V. POWER SYSTEM STUDY MODEL

In this study, a D-STATCOM is used to improve power quality on a 25-kV distribution network. System is composed of two feeders (25 km and 4 km) that transfer power to loads connected at buses B2 and B3, a 25 kV, 60 Hz generation system, a shunt capacitor connected to bus B2 in order to power factor correction at bus B2. Single line diagram of the test system for DSTATCOM and loads that connected to transmission line through a two winding 25kV/630V, △ Y transformers are shown in Figure 8.

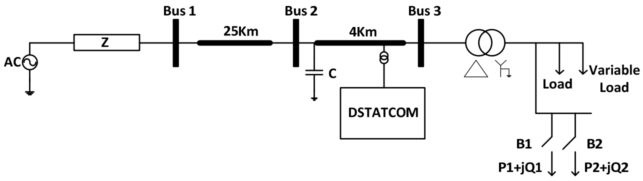


Figure 8. Power system study with DSTATCOM

VI. DSTATCOM CONTROLLER OPERATION

Figure 9 shows Matlab/Simulink model of five-level cascade h-bridge inverter based DSTATCOM. Subsystem of the DSTATCOM controller is shown in Figure 10. The DSTATCOM controller will be designed to compensate reactive power, voltage flicker and mitigate harmonics currents of the load in the Bus 3. The DSTATCOM kept a constant bus B3 voltage by absorbing or generating reactive power [18]. This reactive power transfer is done through the leakage reactance of the coupling transformer by generating a secondary voltage in phase with the grid side voltage [19].

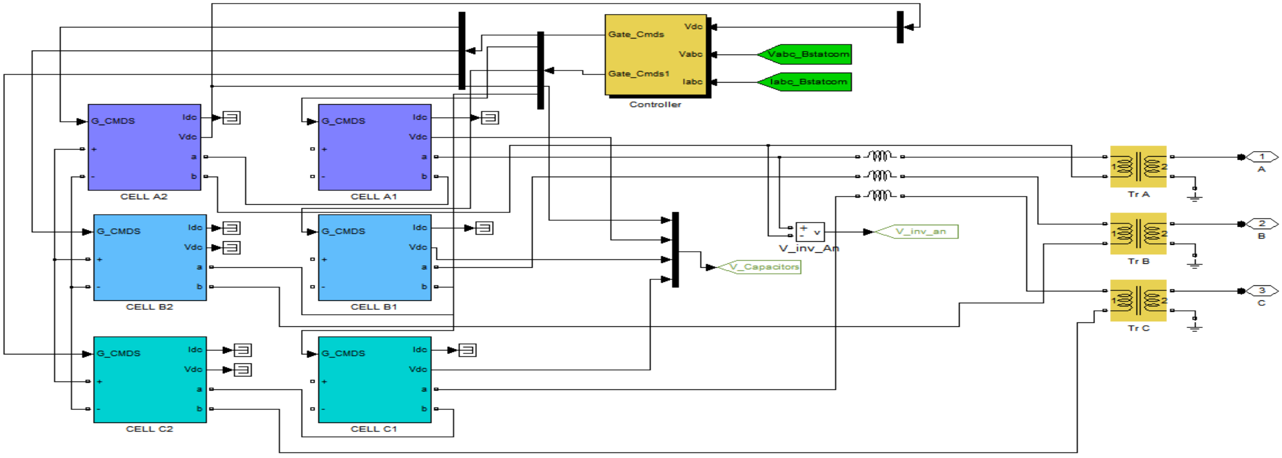


Figure 9. Matlab/Simulink model of five level cascades H-bridge based DSTATCOM

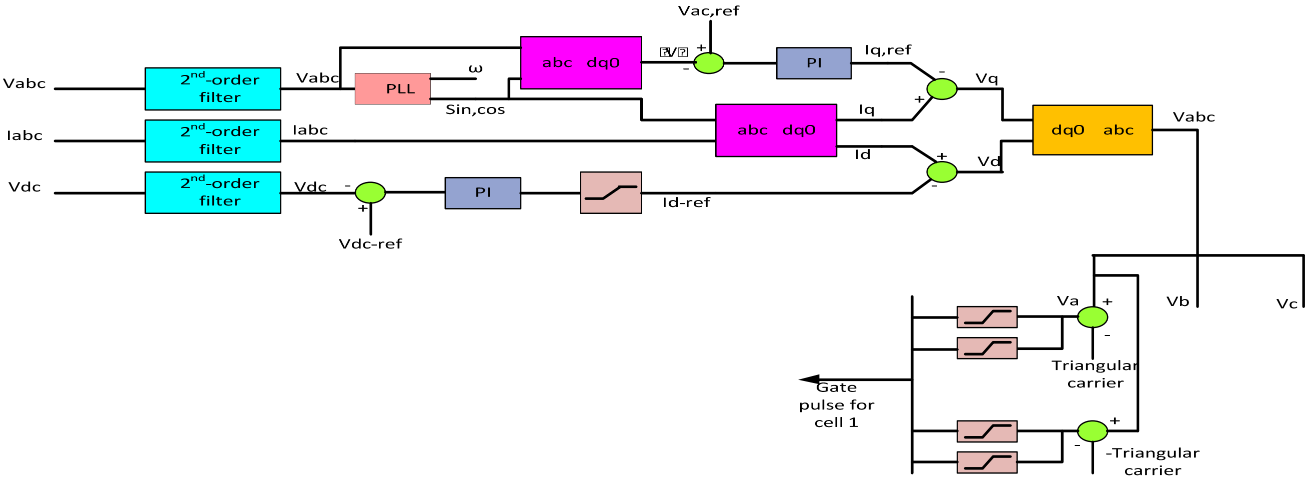


Figure 10. Subsystem of the DSTATCOM controller

This voltage is provided by a voltage-sourced PWM inverter. $V_{a,b,c}$, $I_{a,b,c}$ and I_{dc} are considered as the main controller inputs. The PLL is synchronized to the fundamental of the transformer primary voltages in order to production the angular velocity (ω) and ($\sin\omega, \cos\omega$) vectors [18].

By using ($\sin\omega, \cos\omega$) vectors and $I_{a,b,c}$ as inputs for abc-dq0 transformation block can calculate the d-axis and q-axis components of the voltages and currents. The $I_{q,ref}$ and $I_{d,ref}$ respectively comes from the comparing ($|V|, V_{ac,ref}$) and ($V_{dc}, V_{dc,ref}$).

This structure consists of two proportional-integral (PI) controllers that control the d-axis and q-axis currents. The PI controllers outputs are the V_d and V_q voltages that adapted into phase voltages V_a, V_b, V_c which are used to synthesize the PWM voltages. Phase shift PWM modulation is used to generate the pulse switching for cascade H-bridge inverter.

VII. SIMULATION RESULTS

The performance of the DSTATCOM is validated for the chosen distribution network whose single-line diagram is shown in Figure 8. Voltage in netwotk is different in various moments because of the load changes. Generator voltage fluctuations in power system are shown in Figure 11 without DSTATCOM and it fluctuations between 0.9 pu and 1.1 pu.

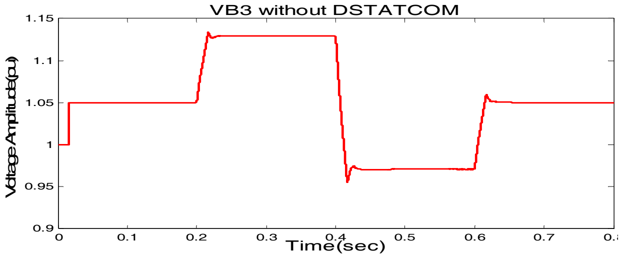


Figure 11. Voltage fluctuations in power system without DSTATCOM

DSTATCOM‘s duty is to exchange reactive power with network in order to keep bus 3’s voltage in 1 pu. Figure 12 illustrates the voltage fluctuations in power system with DSTATCOM that has very few fluctuations. While voltage is more than 1 pu in bus 3, the DSTATCOM absorbs reactive power, moreover, while the voltage is lower than 1 pu, it produces reactive power. Voltage and current fluctuations at bus 3 that loads are connected to it shown in Figure 13.

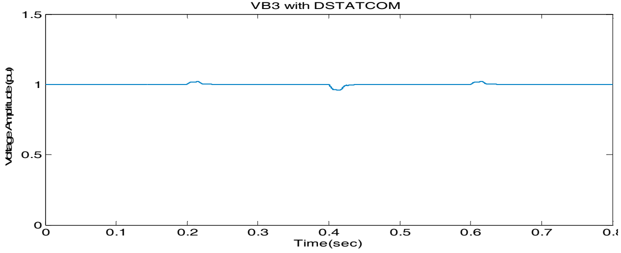


Figure 12. Voltage fluctuations in power system with DSTATCOM

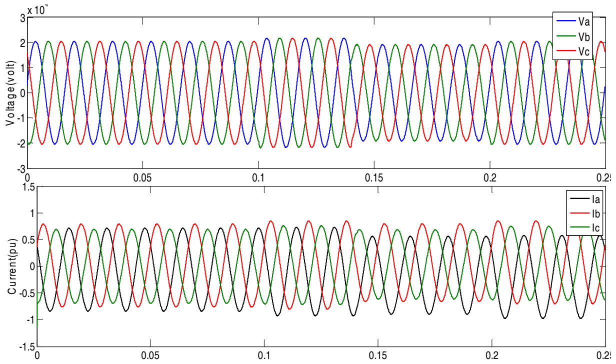


Figure 13. Voltage and current variations without DSTATCOM

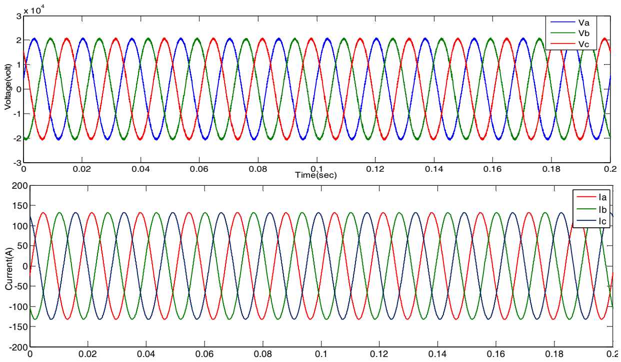


Figure 14. Voltage and current variations with DSTATCOM

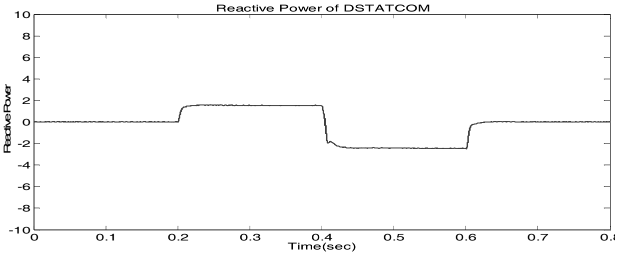


Figure 15. Reactive power exchange between DSTATCOM and grid

By adding a DSTATCOM to near the loads can use it for power quality improvement. Figure 14 shows that voltage and current fluctuations at bus 3 with DSTATCOM. Figure 15 shows reactive power variation in DSTATCOM.

Exchange reactive power between DSTATCOM and grid causes that the power system voltage and current at the consumer side to be balanced. Factor that causes the reactive power exchange between DSTATCOM and grid be done is vertical component of reactive current (I_q). Figure 16 shows how I_q and I_{qref} change.

For adjusting I_q in a needed amount, it is necessary to control amplitude and phase of voltage and injected current to the power system by DSTATCOM. This amplitude control is done by modulation index and Figure 17 illustrates variations of modulation index. The amount of injected voltage and current of DSTATCOM for phase A is shown in Figure 18. Line-neutral output voltage of five-level cascade H-bridge inverter before being filtered is shown in Figure 19. Figure 20 illustrates variations of capacitor voltage used in one of the multilevel inverter cells.

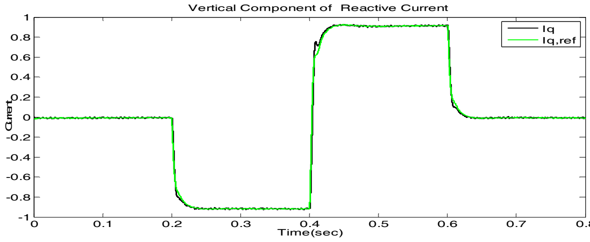


Figure 16. I_q and I_{qref} variations

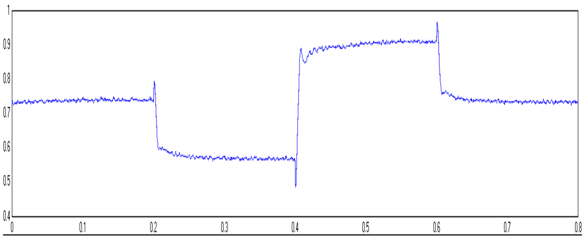


Figure 17. Variations of modulation index

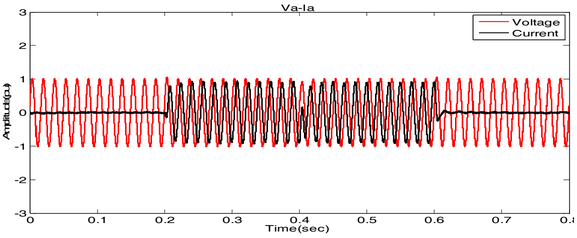


Figure 18. Voltage and current phase A

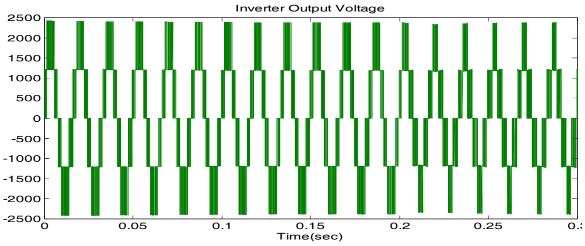


Figure 19. Output voltage of multilevel inverter

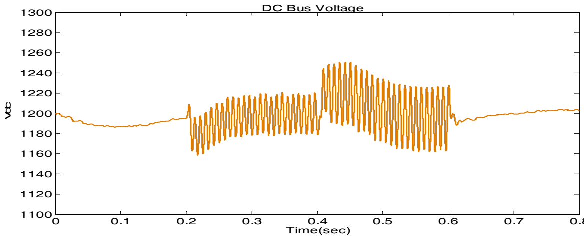


Figure 20. Voltage fluctuations in the dc link capacitors

Figure 21 shows output current harmonic that obtained in the low switching frequencies. In this paper, switching frequency considered of 1800 Hz. As shown in Figure 21 the Total Harmonic Distortion (*THD*) of five-level cascade H-bridge inverter output current before filtering was obtained 1.11%.

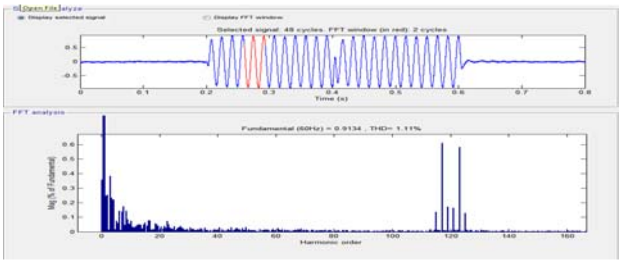


Figure 21. *THD* of multilevel inverter output current

VIII. CONCLUSIONS

In this paper, a DSTATCOM based five-level CHB inverter in order to improve the power quality is studied. The advanced phase shift pulse width modulation technique is used for five-level CHB inverter. In this study, a voltage change every moment in the consumer side but DSTATCOM was able to keep the voltage consumer side in 1 pu. The controller that is used in DSTATCOM is a simple and popular one and it compares i_q and i_d with their original amounts in order to produce V_d and V_q. The *THD* of inverter output current was achieved in the low switching frequency. Simulation results show that the proposed DSTATCOM is very suitable for reactive power compensation and voltage stability.

NOMENCLATURES

V_{dc} : Capacitor or DC link voltage
m : Number of cells
m_f : Frequency modulation index
m_a : Amplitude modulation index
φ_{cr} : Phase shift between two adjacent carrier waves
f_m : Fundamental signal frequency
f_{cr} : Carrier signal frequency
$V_{control}$: Amplitude of the control signal
V_{tri} : Amplitude of the triangular signal
V_s : Secondary voltage of transformers
V_i : Primary voltage of transformers
X : Reactance of coupling inductance
δ : Phase angel between fundamental voltage of DSTATCOM and AC grid

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