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# COMPARATIVE STUDY THD AND AMPLITUDE OUTPUT VOLTAGE VIA INVERTED SINUSOIDAL PULSE WIDTH MODULATION TECHNIQUES FOR NINE LEVEL DIODE CLAMPED MULTILEVEL INVERTER

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**Abstract-** The multilevel inverters have become more popular during the recent years. The multilevel inverters are applied in many industrial applications such as static VAR compensators, AC power supplies, drive systems, active power filters, etc. The topologies of multilevel inverter have several advantages such as low distortion in output voltage with relative low switching frequency, low harmonic and good Electro-Magnetic Interference (EMI). Different pulse width modulation strategies have been used in multilevel inverter topologies. In this paper, various Inverted Sinusoidal Pulse Width Modulation (ISPWM) techniques that compared a sinusoidal reference wave with sinusoidal carrier signal are suggested for a nine-level Diode Clamped Multilevel Inverter (DCMLI) in order to minimize the Total Harmonic Distortion (*THD*) and increase the output voltage. In this study, three strategies will be addressed which are widely used to control of multilevel inverters: Constant Switching Frequency Inverted Sinusoidal Pulse Width Modulation (CSF-ISPWM), Phase Shifted Inverted Sinusoidal Pulse Width Modulation (PS-ISPWM) and Variable Switching Frequency Inverted Sinusoidal Pulse Width Modulation (VSF-ISPWM). The effectiveness of each method is verified through Matlab/Simulink software.

**Keywords:** Diode Clamped Multilevel Inverter, Total Harmonic Distortion, Inverted Sinusoidal Pulse Width Modulation Techniques, CSF Modulation, VSF Modulation, PS Modulation.

## I. INTRODUCTION

According to patents the first multilevel inverters has been designed since 1975. The first topology introduced was the Cascade H-Bridge (CHB) design. This was followed by the Diode-Clamped Inverter which utilizes a series capacitors bank to divide the DC bus voltage. The Flying-Capacitor (FC) topology followed diode-clamped after few years [1]. Multilevel Inverters are becoming popular for their high voltage operating capability in high power applications because of their ability to generate staircase output voltage close to a sinusoidal waveform with lower harmonic distortion, higher output voltage levels and reduce switching losses which can make amends Electro-Magnetic Interference (EMI) problem.

By increase the voltage levels that specifications of conductors and switches are improved, benefits of the use of multilevel inverters are overused and the output *THD* approaches to zero. Various multilevel PWM methods have been proposed during the past two decades. A sinusoidal reference signal is compared to a triangular waveform to generate switching signals of inverter in PWM technique. Recently, researchers have been working on new methods of modulation. One of these new modulation schemes that have attracted much attention is ISPWM method [2]. The Difference between two above-mentioned methods are in carrier wave. In the ISPWM technique carrier waves are sinusoidal.

In this paper, constant switching frequency ISPWM, phase-shifted ISPWM and variable switching frequency ISPWM techniques are discussed. Sub-harmonic Inverted sinusoidal pulse width modulation and switching frequency optimal Inverted sinusoidal pulse width modulation are two techniques of above methods which respectively minimize *THD* and enhance the output voltages [3, 19].

## II. DIODE-CLAMPED MULTILEVEL INVERTER

The neutral point inverter proposed by Nabae, Takahashi, and Akagi in 1981 was essentially a three-level diode-clamped inverter. The main concept of this inverter is to use diodes to limit the power devices voltage stress [4]. The diode-clamped multilevel inverter uses capacitors in series to divide up the dc bus voltage into a set of voltage levels. The voltage over each capacitor and each switch is $V_{dc}$. An $n$ level inverter needs $(n-1)$ voltage sources, $2(n-1)$ switching devices and $(n-1)(n-2)$ diodes. In Figure 1, a three-phase nine-level diode-clamped inverter is shown.

Table 1 lists the output voltage levels possible for one phase of the inverter with the negative dc bus voltage $V_0$ as a reference. State condition 0 means the switch is off, and 1 means the switch is on. Each of the three phases of the inverter shares a common dc bus, which has been subdivided by eight capacitors into nine levels. Each phase has eight complementary switch pairs such

that turning on one of the switches of the pair require that the other complementary switch be turned off [5].

The complementary switch pairs for phase leg $A$ are: $(S_{a1},S'_{a1})$, $(S_{a2},S'_{a2})$, $(S_{a3},S'_{a3})$, $(S_{a4},S'_{a4})$, $(S_{a5},S'_{a5})$, $(S_{a6},S'_{a6})$, $(S_{a7},S'_{a7})$, $(S_{a8},S'_{a8})$. By changing the condition of each pair of switches adds or subtracts one voltage level at the inverter branch output. In order to assure the voltage balance and the output voltage level, the $S_x(n+1)$ switch must open when $S_x(n)$ is switched off, and the $S_x(n-1)$ switch must be conducting when $S_x(n)$ is switched on.

The DCMLI structure has an inherent unbalancing problem among its dc-link capacitors [6]. This is because that the currents $I_1$ and $I_2$ have nonzero average values. This results in the asymmetry between charging and discharging times of the capacitors causing overcharging or undercharging of each capacitors with a constant dc voltage $V_{dc}$. A single leg cannot face this problem because there are no intra-phase redundant states to use for this purpose. In other word, multi-phase diode-clamped inverter can balance the capacitors voltages using joint-phase redundant states. Figure 2 shows, phase to neutral voltage waveforms for a nine-level DCMLI. The line- neutral voltage $V_a$ consists of a phase-leg $A$ voltage and neutral point. This means that an $m$-level diode-clamped inverter has an $m$-level output phase voltage and a $(2m-1)$-level output line voltage.

As shown in Figure 2, a multilevel inverter can produce quarter-wave symmetric voltage waveform synthesized by several dc voltages.

Table 1. Output voltage levels and switching mode for phase A

| $V_{ao}$ | $S_{a8}$ | $S_{a7}$ | $S_{a6}$ | $S_{a5}$ | $S_{a4}$ | $S_{a3}$ | $S_{a2}$ | $S_{a1}$ | $S'_{a8}$ | $S'_{a7}$ | $S'_{a6}$ | $S'_{a5}$ | $S'_{a4}$ | $S'_{a3}$ | $S'_{a2}$ | $S'_{a1}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $+4V_{dc}/8$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $+3V_{dc}/8$ | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $+2V_{dc}/8$ | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| $+V_{dc}/8$ | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| $-V_{dc}/8$ | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| $-2V_{dc}/8$ | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| $-3V_{dc}/8$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| $-4V_{dc}/8$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

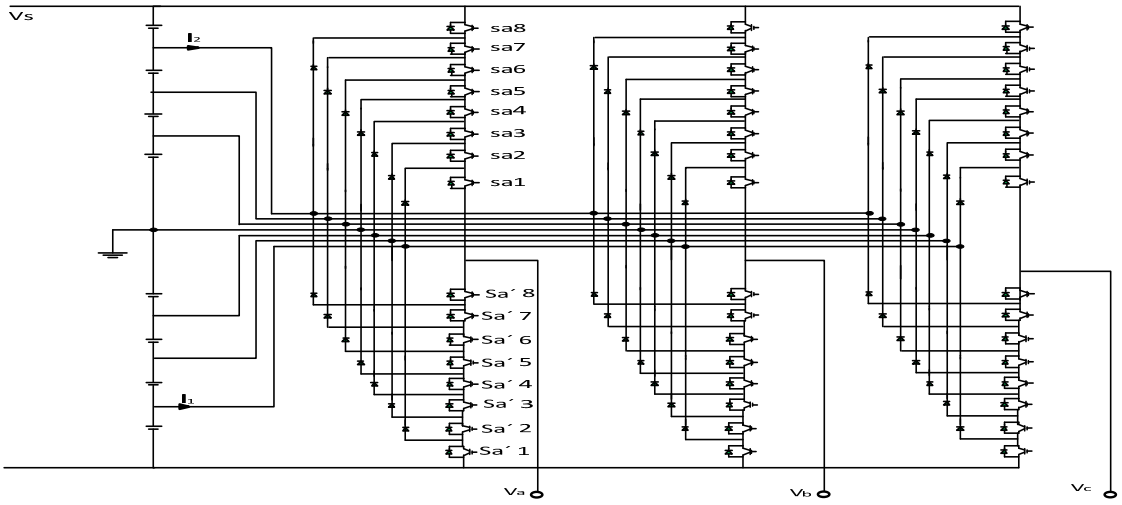



Figure 1. A three-phase nine-level diode clamped inverter

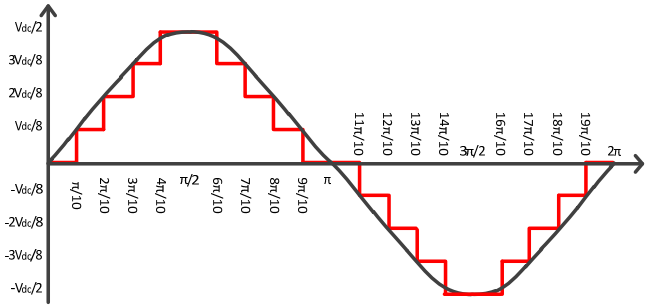



Figure 2. Line-neutral voltage waveforms nine level DCMLI

One application of the multilevel diode-clamped inverter is an interface between a high-voltage dc transmission line and an ac transmission line. Another application would be as a variable speed drive for high-power medium-voltage (2.4 kV to 13.8 kV) motors as proposed in [7, 18]. Static VAR compensation is an additional function for which several authors have proposed for the diode-clamped inverter. The principal advantages and disadvantages of multilevel diode-clamped converters are as follows:

Advantages:

- Switching frequency can be low.
- Reactive current and negative-phase-sequence current can be controlled.
- The capacitors can be pre-charged as a group.
- Simple control method for back-to-back power transfer system.

Disadvantages:

- Difficulties with active power flow.
- Real power flow is difficult for a single inverter because the intermediate dc levels will tend to overcharge or discharge without accurate monitoring and control.

## III. MODULATION TECHNIQUE

According to switching frequency, multilevel inverter modulation is basically classified in two groups of methods: modulation with fundamental switching frequency and high switching frequency PWM. The classification of PWM multilevel inverter modulation strategies have shown in Figure 3. In recent years, numerous researchers which have been done about multilevel sinusoidal PWM, multilevel space vector PWM and selective harmonic elimination strategies [8].

In this paper, the authors have focused on the multilevel Inverted Sinusoidal PWM (ISPWM) strategies. The advantages of the ISPWM method are:

- Harmonics of carrier frequencies or its multiples are not produced.
- The ISPWM strategy improves the fundamental output voltage particularly at lower modulation index ranges.
- The noticeable improvement in the total harmonic distortion in the lower range of modulation index attracts drive applications where low speed operation is required.

Previous authors have extended several different two-level multilevel carrier-based PWM techniques as a means for controlling the active devices in a multilevel inverter [9]. The ISPWM method uses a sinusoidal reference signal and an inverted sine carrier. In the gating pulse generation of the proposed ISPWM, the triangular carrier waveform of PWM is replaced by an inverter sine waveform.

In this paper, three major ISPWM techniques have been discussed in order to compare the *THD* and amplitude of output voltage in a nine level DCMLI.
The techniques are:

- Constant switching frequency PWM
- Variable switching frequency PWM
- Phase-shifted PWM

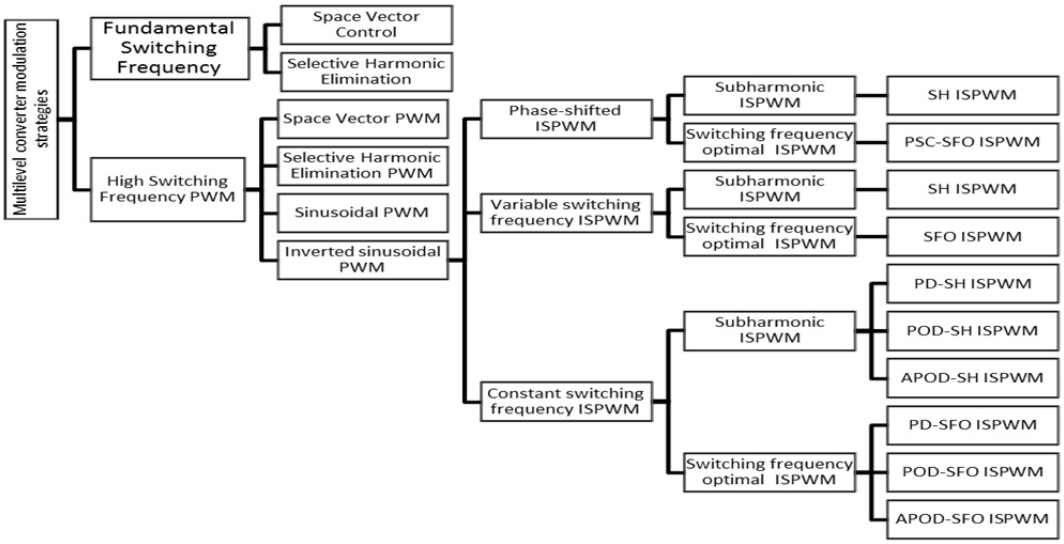



Figure 3. The classification of PWM multilevel inverter modulation strategies

## IV. CONSTANT SWITCHING FREQUENCY ISPWM

### A. Sub-Harmonic ISPWM

Carrara extended SH-PWM to multiple levels as follows [10]: The constant switching frequency pulse-width modulation technique is most popular and very simple switching schemes. For $m$-level inverter, $m-1$ carriers with the same frequency $f_c$ and the same amplitude $A_C$ are disposed such that the bands they occupy are contiguous. The reference waveform has peak-to-peak amplitude $A_m$, the frequency $f_m$ and it is zero centered in the middle of the carrier set.

The reference is incessantly compared with each of the carrier signals. If the reference is greater than a carrier signal, then the active device conforming to that carrier is switched on and if the reference is less than a carrier signal, then the active device conforming to that carrier is switched off. The frequency modulation index $m_f$, which is the ratio of carrier frequency to modulating signal frequency, is expressed by equation:

$$m_f = \frac{f_c}{f_m} \tag{1}$$

In multilevel inverters, the amplitude modulation index $m_a$ defined as:

$$m_a = \frac{A_m}{(m-1)A_c} \quad (2)$$

The advantages of this method are as follows:

- it has lower *THD*.
- it is easily applied to any multilevel inverter.
- Increase the output voltage amplitude.

The SH-ISPWM method has serious disadvantages such as:

- lower fundamental component
- lower voltage modulation index

In multilevel case, Sub-Harmonic ISPWM (SH-ISPWM) techniques with three different disposed sinusoidal carriers [9, 11] were proposed as follows:

- Phase Disposition Inverted Sinusoidal Pulse-Width Modulation (PD-ISPWM), where all the carriers are in phase.
- Phase Opposition Disposition Inverted Sinusoidal Pulse-Width Modulation (POD-ISPWM), where all the carriers above the zero value reference are in phase among them, but in opposition with those below.
- Alternative Phase Opposition Disposition Inverted Sinusoidal Pulse-Width Modulation (APOD-ISPWM), where each carrier band is shifted by 180° from the nearby bands.

Figure 4 illustrates three major constant switching frequency for sub-harmonic ISPWM techniques: PD-SH-ISPWM, POD-SH-ISPWM and APOD-SH-ISPWM. As shown in Figure 4(a), in PD-SH-ISPWM technique all sinusoidal carrier in phase and compared with sinusoidal reference signal. Figures 4(b) and 4(c) show POD-SH-ISPWM and APOD-SH-ISPWM techniques, respectively. As can be seen in Figure 4(b) and 4(c), the reference signals have some margin at unity amplitude modulation index.

### B. Switching Frequency Optimal ISPWM

This method was presented by Menzies [12]. Triples harmonic voltage is added to refrence waveforms in the Switching Frequency Optimal Inverted Sinusoidal Pulse-Width Modulation (SFO-ISPWM) method. This method consists of the instantaneous average of the minimum and maximum of the three reference voltages $(V_a, V_b, V_c)$ and subtracts this value from each of the unique reference voltages to obtain the modulation waveforms.

$$V_{offset} = \left\{ \frac{\max(V_a, V_b, V_c) + \min(V_a, V_b, V_c)}{2} \right\} \quad (3)$$

$$\begin{aligned} V_{aSFO} &= V_a - V_{offset} \\ V_{bSFO} &= V_b - V_{offset} \\ V_{cSFO} &= V_c - V_{offset} \end{aligned} \quad (4)$$

The ability of SFO-ISPWM technique to product the zero-sequence restricts its use to a three-phase three-wire system, but it enables the modulation index to be increased by 15% before pulse dropping occurs [9, 13]. In the switching frequency optimal method carrier waves are placed in relation to the reference in three situations:

- Phase Disposition Inverted Sinusoidal Pulse-Width Modulation (PD-SFO-ISPWM), where all the carriers are in phase.
- Phase Opposition Disposition Inverted Sinusoidal Pulse-Width Modulation (POD-SFO-ISPWM), where all the carriers above the zero value reference are in phase among them, but in opposition with those below.
- Alternative Phase Opposition Disposition Inverted Sinusoidal Pulse-Width Modulation (APOD-SFO-ISPWM), where each carrier band is shifted by 180° from the nearby bands.

In switching frequency optimal ISPWM method triples harmonic voltage is added to sinusoidal refrence waveforms. Figure 5 illustrates three major constant switching frequencies for switching frequency optimal ISPWM techniques: PD-SFO-ISPWM, POD-SFO-ISPWM and APOD-SFO- ISPWM.

Figures 4(a), 4(b) and 4(c) show PD-SFO-ISPWM, POD-SFO-ISPWM and APOD-SFO-ISPWM techniques, respectively. As can be seen in Figure 5(a) all carrier in phase but in Figure 5(b) the carriers above the zero reference are in phase and in Figure 5(c) each carrier band is shifted by 180° from the adjacent bands.

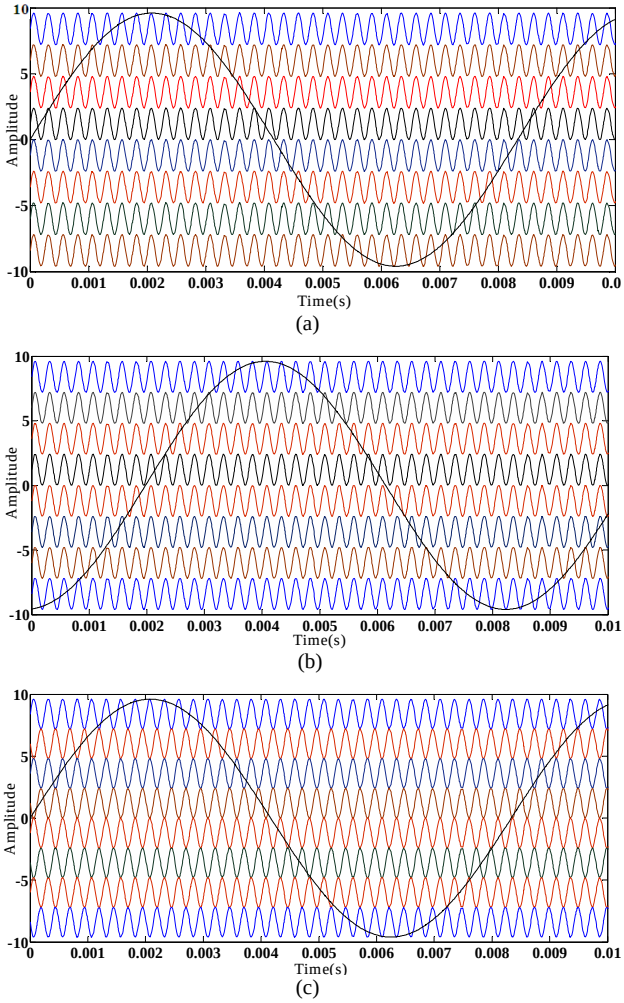



Figure 4. Sub-harmonic ISPWM technique in constant switching frequency state for nine-level diode clamped inverter
(a) PD-ISPWM, (b) POD ISPWM, (c) APOD ISPWM

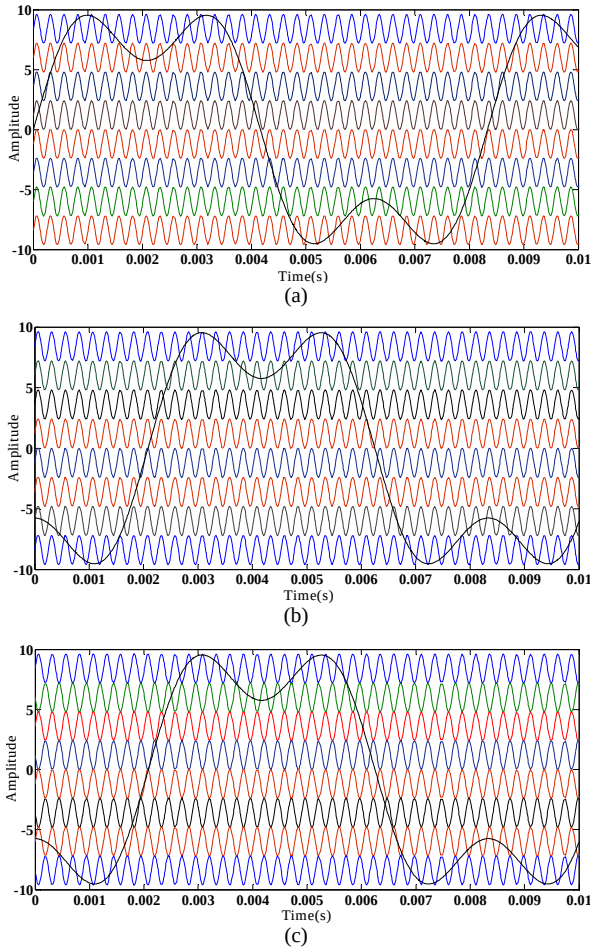



Figure 5. Switching frequency optimal ISPWM in constant switching frequency state for nine-level diode clamped inverter
(a) PD-ISPWM, (b) POD ISPWM, (c) APOD ISPWM

## V. VARIABLE SWITCHING FREQUENCY ISPWM

### A. Sub-Harmonic ISPWM

For a multilevel inverter, if the level is $m$ there will be $(m-1)$ carrier set with variable switching frequency pulse width modulation when compared with third harmonic injection reference [14]. The carriers are in phase across for all the bands. In this technique, significant harmonic energy is localized at the carrier frequency. Since, it is a co-phrasal component; it doesn't appear line to line voltage. In this study we proposed a nine level DCMLI inverter which levels are $0$, $\pm\frac{V}{8}$, $\pm\frac{2V}{8}$, $\pm\frac{3V}{8}$, $\pm\frac{V}{2}$ which is assigned to have variable switching frequency of 2 KHz and 5 KHz as shown in Figure 6. As it is seen in Figure 6 upper and lower carrier have the same frequency (2 KHz) and the other carriers in a phase and have the same frequency that is 5 KHz.

### B. Switching Frequency Optimal ISPWM

For a nine level multilevel inverter, 8 carrier sets with variable switching frequency carrier pulse-width modulation when compared with third harmonic injection reference. For third harmonic injection given as [9, 15]:

$$Y = 1.15\sin\theta + \frac{1.15}{6}\sin 3\theta \quad (5)$$

The resulting flat topped waveform lets over modulation while maintaining excellent AC term and DC term spectra. This is a suggested approach to amend the output voltage without entering the over modulation range. So any carriers used for this reference will improve the output voltage by 15% without increasing harmonics. In this study we proposed a nine level DCMLI inverter which levels are $0$, $\pm\frac{V}{8}$, $\pm\frac{2V}{8}$, $\pm\frac{3V}{8}$, $\pm\frac{V}{2}$ which is assigned to have variable switching frequency of 2 KHz and 5 KHz as shown in Figure 7. As can be seen in figure 6 upper and lower carrier have the same frequency (2 KHz) and the other carriers in a phase and have the same frequency that is 5 KHz and triples harmonic voltage is added to sinusoidal reference waveforms.

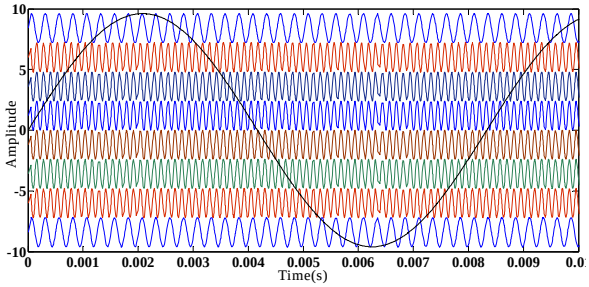



Figure 6. Variable switching frequency sub-harmonic ISPWM method for nine-level DCMLI

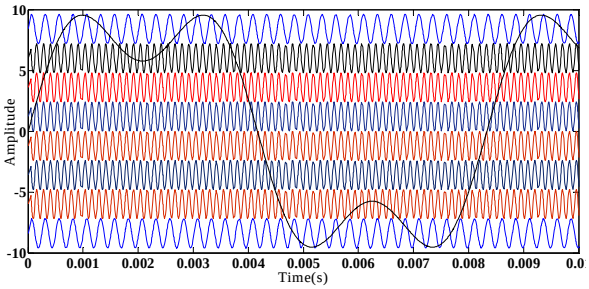



Figure 7. Variable switching frequency optimal ISPWM method for nine-level DCMLI

## VI. PHASE-SHIFTED ISPWM

In Phase Shifted Inverted sinusoidal Pulse Width Modulation the frequency of the all the sinusoidal carrier waves are kept constant and it is phase shifted by each other [16]. This method subdivided in to Phase Shifted Sub-Harmonic Inverted Sinusoidal Pulse Width Modulation (PS-SH-ISPWM) and Phase Shifted Switching Frequency Optimal Inverted Sinusoidal Pulse Width Modulation (PS-SFO-ISPWM).

### A. Sub-Harmonic ISPWM

Phase-Shifted Sub-Harmonic ISPWM has shows in Figure 8. Gating pulses are generated by comparing sinusoidal reference signal with sinusoidal carriers. Phase shifting carrier for diode clamped multilevel inverter is given by $\pi/m$ where, $m$ is the level of diode clamped inverter. In other words, in this article, phase difference between successive carriers wave is 22.5°.

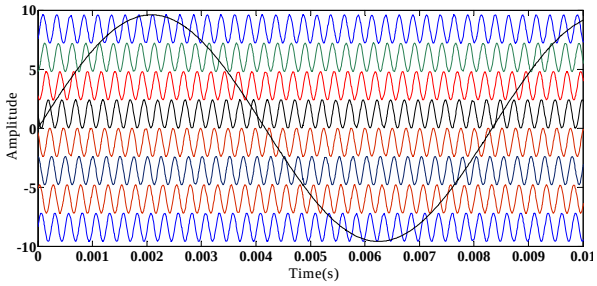



Figure 8. Phase shift sub-harmonic ISPWM for nine-level DCMLI

### B. Switching Frequency Optimal ISPWM

The proposed control strategy replaces the prevalent constant frequency carrier waveform by variable frequency inverted sine wave [17]. This method was presented by Menzies. Triples harmonic voltage is added to each of the carrier waveforms in the Switching Frequency Optimal Inverted Sinusoidal Pulse Width Modulation (SFO-ISPWM) method. This method consists of the instantaneous average of the minimum and maximum of the three reference voltages $(V_a, V_b, V_c)$ and subtracts this value from each of the unique reference voltages to obtain the modulation waveforms.

$$V_{offset} = \left\{ \frac{\max(V_a, V_b, V_c) + \min(V_a, V_b, V_c)}{2} \right\}$$

$$V_{aSFO} = V_a - V_{offset}$$

$$V_{bSFO} = V_b - V_{offset}$$

$$V_{cSFO} = V_c - V_{offset}$$

The ability of SFO-ISPWM technique to product the zero-sequence limits its use to a three-phase three-wire system, but it enables the modulation index to be increased by 15% before pulse dropping occurs. The inverted Sinusoidal PWM has a better spectral quality and a higher fundamental voltage compared to the triangular based PWM, but the main disadvantage is the marginal increase in the magnitude of lower order harmonics and unbalanced switch utilization. This is overcome by employing variable frequency inverted sine carrier signals. Phase shift switching frequency optimal ISPWM show in Figure 9.

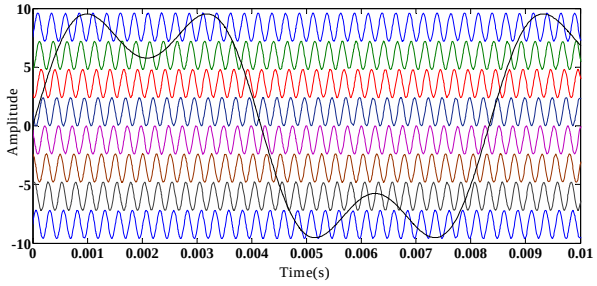



Figure 9. Phase shift switching frequency optimal ISPWM for nine-level DCMLI

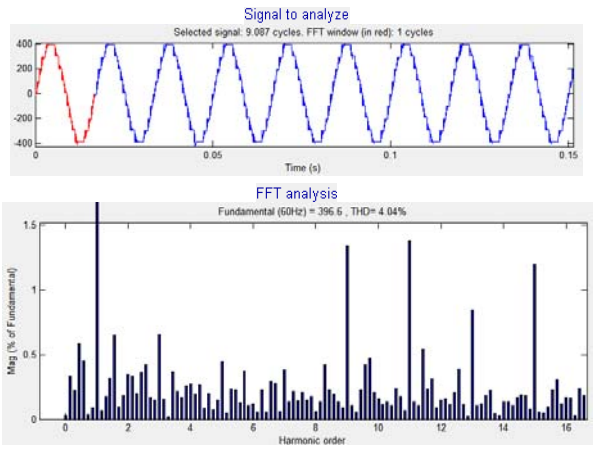
## VII. SIMULATION RESULT

In this paper three different ISPWM methods such as constant switching frequency inverted sinusoidal pulse width modulation, variable switching frequency inverted sinusoidal pulse width modulation and phase shifted inverted sinusoidal pulse width modulation In order to compare the *THD* and output voltage level in a nine-level DCMLI inverter used. Figure 10 illustrates the one phase output voltage and the *THD*. Table 2 has presented in order to make better comparison of the above-mentioned methods. Parameters used in simulations for all methods: $V_{dc} = 100\ V$, $m_a = 0.8$, $f_m = 60$ Hz and $f_c = 25000$ Hz

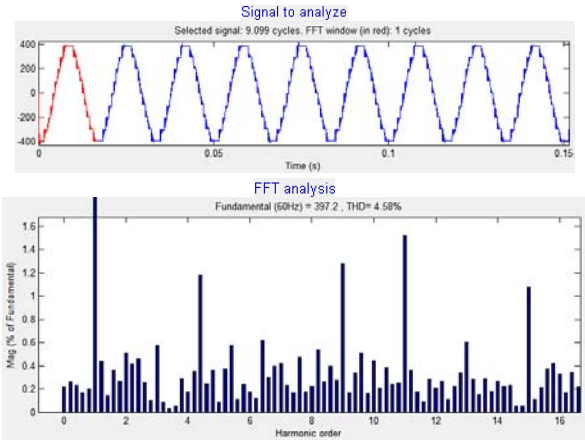
As shown in Figure 10, when the modulation is based on switching frequency optimal method, *THD* rate rises sharply. Using the sub-harmonic method has smaller rate of *THD* compared with switching frequency optimal. Third-order harmonic injection to the reference wave, as expected increases the DCMLI output voltage *THD*. Not only Usage of phase shift sub-harmonic ISPWM can provide the lowest range of *THD*, but also increases amount of output voltage.

Table 2. Output voltage and *THD* for constant switching frequency ISPWM, variable switching frequency ISPWM and phase-shifted ISPWM

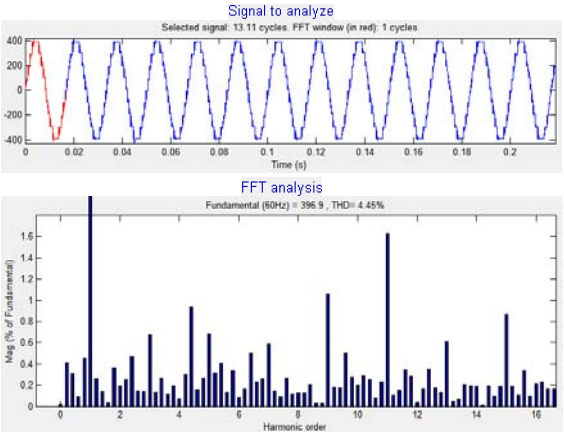
| Modulation Method | *THD*% | Output Voltage (V) |
|---|---|---|
| Constant Switching Frequency (PD SH ISPWM) | 4.04 | 396.6 |
| Constant Switching Frequency (POD SH ISPWM) | 4.58 | 397.2 |
| Constant Switching Frequency (APOD SH ISPWM) | 4.45 | 396.9 |
| Constant Switching Frequency (PD SFO ISPWM) | 38.89 | 406.2 |
| Constant Switching Frequency (POD SFO ISPWM) | 38.60 | 408.5 |
| Constant Switching Frequency (APOD SFO ISPWM) | 39.30 | 407 |
| Variable Switching Frequency (SH ISPWM) | 4.03 | 403.2 |
| Variable Switching Frequency (SFO ISPWM) | 34.44 | 402.4 |
| Phase Shifted (SH ISPWM) | 3.94 | 406.8 |
| Phase Shifted (SFO ISPWM) | 34.64 | 421.2 |



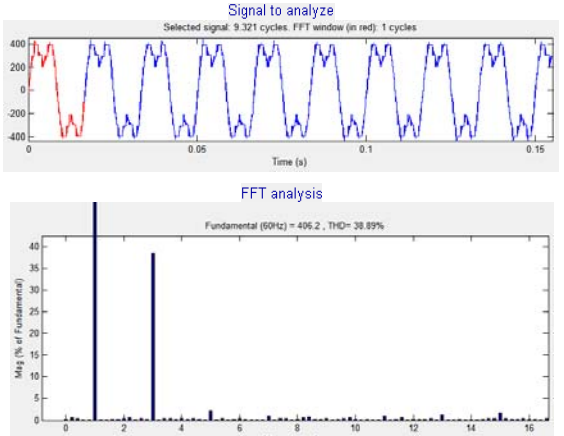

(a)


Signal to analyze
Selected signal: 9.099 cycles. FFT window (in red): 1 cycles
Time (s)
FFT analysis
Fundamental (60Hz) = 397.2 , THD= 4.58%
Mag (% of Fundamental)
Harmonic order

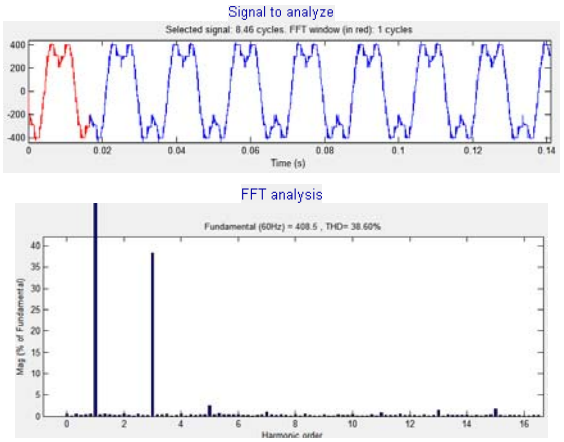
(b)


Signal to analyze
Selected signal: 13.11 cycles. FFT window (in red): 1 cycles
Time (s)
FFT analysis
Fundamental (60Hz) = 396.9 , THD= 4.45%
Mag (% of Fundamental)
Harmonic order

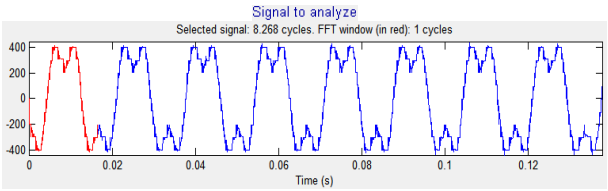
(c)

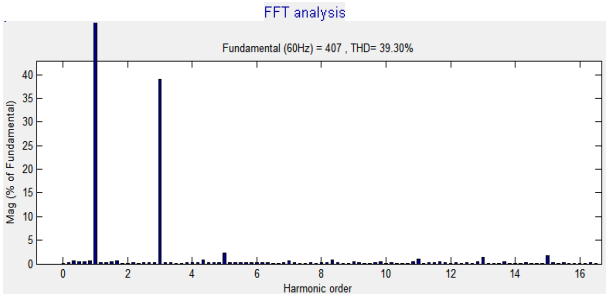

Signal to analyze
Selected signal: 9.321 cycles. FFT window (in red): 1 cycles
Time (s)
FFT analysis
Fundamental (60Hz) = 406.2 , THD= 38.89%
Mag (% of Fundamental)
Harmonic order

(d)

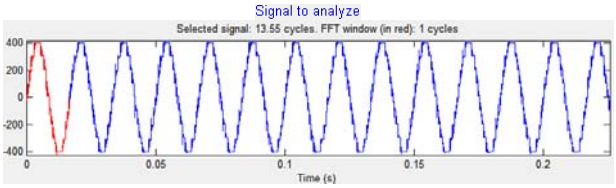

Signal to analyze
Selected signal: 8.46 cycles. FFT window (in red): 1 cycles
Time (s)
FFT analysis
Fundamental (60Hz) = 408.5 , THD= 38.60%
Mag (% of Fundamental)
Harmonic order

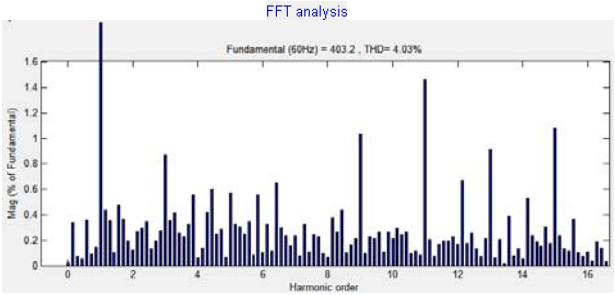
(e)


Signal to analyze
Selected signal: 8.268 cycles. FFT window (in red): 1 cycles
Time (s)

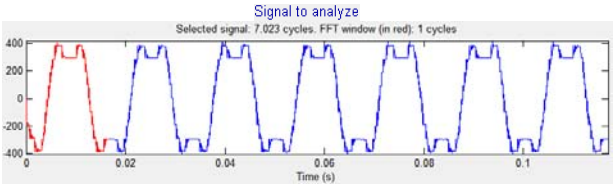

FFT analysis
Fundamental (60Hz) = 407 , THD= 39.30%
Mag (% of Fundamental)
Harmonic order

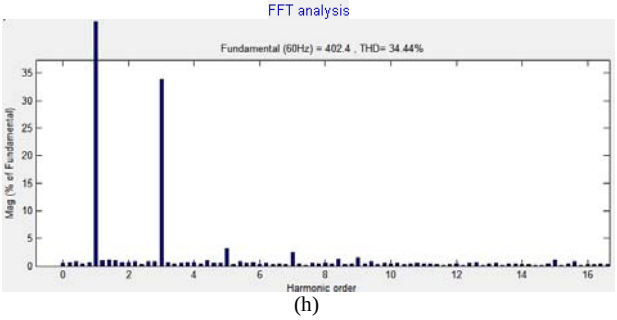
(f)


Signal to analyze
Selected signal: 13.55 cycles. FFT window (in red): 1 cycles
Time (s)

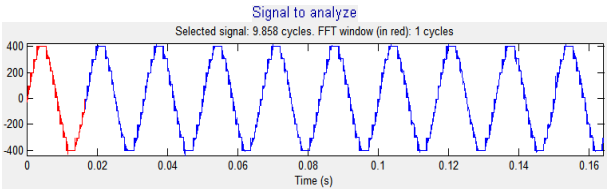

FFT analysis
Fundamental (60Hz) = 403.2 , THD= 4.03%
Mag (% of Fundamental)
Harmonic order

(g)


Signal to analyze
Selected signal: 7.023 cycles. FFT window (in red): 1 cycles
Time (s)


FFT analysis
Fundamental (60Hz) = 402.4 , THD= 34.44%
Mag (% of Fundamental)
Harmonic order

(h)


Signal to analyze
Selected signal: 9.858 cycles. FFT window (in red): 1 cycles
Time (s)

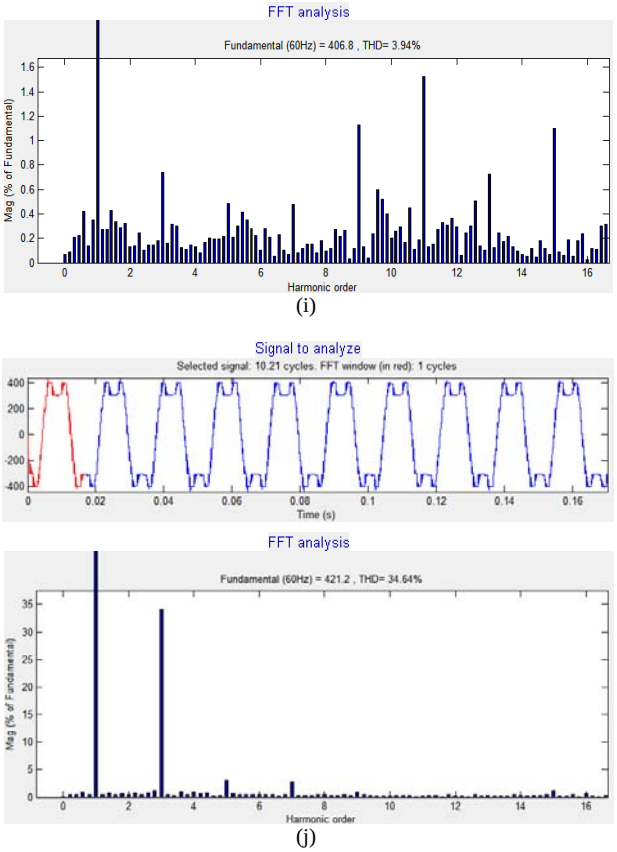



Figure 10. FFT Analyses, (a) CSF PD SH ISPWM, (b) CSF POD SH ISPWM, (c) CSF APOD SH ISPWM, (d) CSF PD SFO ISPWM, (e) CSF POD SFO ISPWM, (f) CSF APOD SFO ISPWM, (g) VSF SH ISPWM, (h) VSF SFO ISPWM, (i) PS SH ISPWM, (j) PS SFO ISPWM

## VIII. CONCLUSIONS

Different modulation methods used in the multilevel inverter structure has caused sharp increase in application of it in industry. By the use of different modulation methods, many specifications in multilevel inverter can be controlled such as *THD* and amplitude output voltage. In this paper several types of modulation based on comparing a sinusoidal refrence waveform with sinusoidal carrier waveform presented. Three general types of modulation which have been studied in this paper are: constant switching frequency ISPWM, variable switching frequency ISPWM, phase-shifted ISPWM. The above methods were examined in order to obtain and compare the *THD* and output voltage amplitude in a nine level dioed clamped inverter. Method phase shift sub-harmonc ISPWM has the best result towards another studied method in this paper.

## NOMENCLATURES

$V_{dc}$ : inverter DC bus voltage

$m$ : level of output voltage or inverter

$I_1$ :common current between 3phase in branch 1

$I_2$ : common current between 3phase in branch 2

$V_{ab}$ : voltage between phase a and b

$f_c$ : carrier frequency

$f_m$ : modulating signal frequency

$A_c$ : carrier amplitude

$A_m$ : modulating signal amplitude

$m_f$ : frequency modulation index

$m_a$ : amplitude modulation index

$V_{offset}$ : the instantaneous average of the minimum and maximum of the three reference voltages

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