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HARMONIC MINIMIZATION IN CASCADED H-BRIDGE MULTILEVEL INVERTER BY ICA

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Abstract- Multilevel inverter is to synthesis the desired output voltage waveform from several steps of voltage and has many advantages than the traditional two level inverter so it is widely used. There are several modulation methods to achieve a sinusoidal output. One of them is Selective Harmonic Elimination (SHE).The main difficulty for this method is to solve nonlinear transcendental equations. So optimization techniques are used to solve them. In this paper, the minimization of harmonics in a Cascaded Multilevel Inverter (CMLI) by considering the equality of separated DC sources by using Imperialistic Competitive Algorithm (ICA) is presented.

Keywords: Cascaded Multilevel Inverter, Selective Harmonic Elimination, Imperialistic Competitive Algorithm (ICA).

I. INTRODUCTION

In recent years, there is a growing demand for high voltage conversion systems capable of providing high output voltage signals and having good spectral performance and easy control. Multilevel converters have attracted increasing attention in medium-voltage and high-power applications. These converters have been widely used in DGs, FACTS devices, HVDC transmission systems, and electric drives for AC motors and active filters [1]. Three different topologies have been proposed for multilevel inverters, diode-clamped (neutral-clamped) [2], capacitor clamped (flying capacitors) [3], and cascaded multilevel with separated DC sources [4].

Most attractive features of multilevel inverters are as:

A- They can generate output voltages with extremely low distortion and lower *dv*/*dt*

B- They draw input current with very low distortion

C- They generate smaller Common-Mode (CM) voltage thus reducing the stress in the motor bearings. In addition, using sophisticated modulation methods, CM voltages can be eliminated

D- They can operate with a lower switching frequency [5]

With an increasing number of DC voltage sources, the converter output voltage waveform approaches a nearly sinusoidal waveform while using a fundamental frequency-switching scheme.

The primary advantage of multilevel inverter is their small output voltage, results in higher output quality, lower harmonic component, better electromagnetic computability, and lower switching losses. In addition, several modulation and control strategies have been developed or adopted for multilevel inverters including the following. Pulse Width Modulation (PWM), Sinusoidal Pulse Width Modulation (SPWM), Space Vector PWM (SVPWM), Carrier-Based PWM, Selective Harmonic Elimination PWM (SHE-PWM), and Space Vector Modulation (SVM) strategies for controlling and determine switching angles to achieve the desired output voltage and eliminating the undesired harmonics.

However, PWM techniques are not able to eliminate lower order harmonics. Another approach is to choose the switching angles so that specific higher order harmonics such as the 5th, 7th, 11th, and 13th are suppressed in the output voltage of the inverter. This method is known as Selective Harmonic Elimination (SHE) or programmed PWM techniques in technical literature. A fundamental problem with such method is to obtain the arithmetic solution of nonlinear transcendental equations, which contain trigonometric terms and naturally present multiple solutions. The main difficulty for selective harmonic elimination method is to compute the switching angles because of nonlinear equations.

Many iterative techniques such as Newton-Raphson method have been reported to solve the nonlinear transcendental equations resulting in only one solution set or multiple solutions by assuming a proper initial guess [6, 9]. Several traditional methods can be used to estimate switching angles, however, a few of them may be computationally expensive. A difficulty with these approaches is that for higher levels of multilevel inverter the order of polynomials become very high, thereby making the computations of solutions of these polynomial equations very complex.

II. CASCADE H-BRIDGE MULTILEVEL INVERTER

The concept of this inverter is based on connecting H-bridge inverters with separate DC sources in series to get a sinusoidal voltage output. The general function of this multilevel inverter is to synthesis a desired voltage

from several Separate DC Sources (SDCSs), which may be obtained from batteries, fuel cells, or ultra-capacitors. The output voltage is the sum of the voltage that is generated by each cell. Each full-bridge can generate three different voltage outputs, $+V_{dc}$, 0, and $-V_{dc}$ by different combinations of the four switches, S_1, S_2, S_3, and S_4.

For example, a 7-level cascaded multilevel inverter with three isolated DC sources and phase voltage waveform of it are shown in Figures 1 and 2, respectively. The number of output voltage levels are $2n+1$, where n is the number of cells or separate DC source. One of the advantages of this type of multilevel inverter is that it needs less number of components comparative to the diode clamped or the flying capacitor, so the price and the weight of the inverter is less than that of the two types. DC sources can be equal or unequal so we have two configurations, symmetric and asymmetric cascade H-bridge multilevel inverter. The switching angles can be chosen in such a way that the total harmonic distortion is minimized [10, 11].

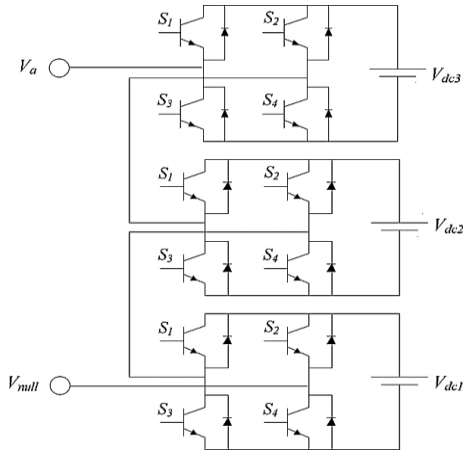


Figure 1. Seven-level cascaded H-bridge multilevel inverter with separate DC sources

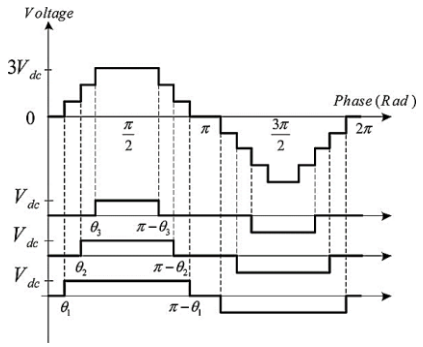


Figure 2. The output voltage waveform of a 7-level inverter

III. SELECTIVE HARMONIC ELIMINATION

Assuming a nine-level symmetric cascade H-bridge inverter, which output waveform shown in Figure 3. For a stepped waveform such as the one depicted in Figure 3 with steps, Fourier transform for this waveform follows:

$$V(\omega t)=\sum_{n=1}^{\infty}V_n\sin(n\omega t) \tag{1}$$

where, V_n are voltage harmonic components, which are introduced in Equation (2).

$$V_n=\begin{cases}\dfrac{4v_{dc}}{n\pi}\displaystyle\sum_{n=1}^{s}\cos(n\theta_i), & n=\text{odd}\\ 0, & n=\text{even}\end{cases} \tag{2}$$

Only odd order harmonics exist due to half cycle symmetry of waveform. It is necessary to eliminate low order harmonics, from 5 to 13. It is not needed to delete triple harmonics because they will be eliminated in three-phase output. The expansion for Equation (2) results in Equation (3).

$$\begin{cases}V_1=\dfrac{4v_{dc}}{\pi}\left[\cos(\theta_1)+\cos(\theta_2)+...+\cos(\theta_4)\right]\\ V_5=\dfrac{4v_{dc}}{5\pi}\left[\cos(5\theta_1)+\cos(5\theta_2)+...+\cos 5(\theta_4)\right]\\ \vdots\\ V_{13}=\dfrac{4v_{dc}}{13\pi}\left[\cos(13\theta_1)+\cos(13\theta_2)+...+\cos(13\theta_4)\right]\end{cases} \tag{3}$$

$$M=\frac{V_1}{4v_{dc}s/\pi} \tag{4}$$

where, M is modulation index. Finally, we can write Equation (3) as follow:

$$\begin{cases}M=\dfrac{1}{4}\left[\cos(\theta_1)+\cos(\theta_2)+...+\cos(\theta_4)\right]\\ 0=\left[\cos(5\theta_1)+\cos(5\theta_2)+...+\cos(5\theta_4)\right]\\ \vdots\\ 0=\left[\cos(13\theta_1)+\cos(13\theta_2)+...+\cos(13\theta_4)\right]\end{cases} \tag{5}$$

For harmonic optimization, switching angles θ_1, ..., θ_4 for a 9-level inverter shown in Figure 3 have to be selected so certain order harmonics are eliminated. It is necessary to determine six switching angles, namely θ_1, ..., θ_4 such that Equation (3) is satisfied. These equations are nonlinear and different solution methods can be applied to them. This set of nonlinear equations can be solved by iterative techniques such as the Newton-Raphson method [12]. However, such techniques need a good initial guess, which should be very close to the exact solution patterns.

Therefore, the Newton-Raphson method is not feasible to solve the SHE problem for a large number of switching angles if good initial guesses are not available. To solve the SHE problem another approach based on mathematical theory of resultant is proposed, where the SHE problem are converted into an equivalent set of polynomial equations and then the mathematical theory of resultant is utilized to find all possible sets of solution.

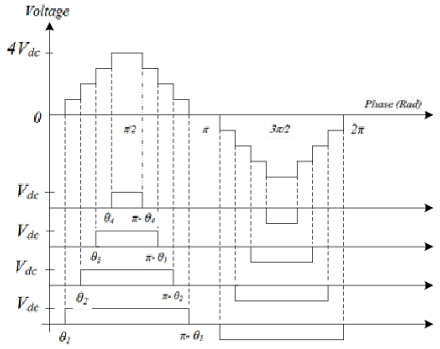


Figure 3. The output voltage waveform of a 9-level inverter

However, this approach appears to be unattractive because as the number of inverter level increases, so does the degree of the polynomials of the mathematical model. This is likely to lead to numerical difficulty and substantial computational burden as well [13]. GA and PSO algorithms have been used for this aim [14, 15]. In this paper, the Imperialistic Competitive Algorithm (ICA) approach is developed to deal with the SHE problem with equal DC sources.

IV. ICA ALGORITHM

Figure 4 shows the flowchart of the ICA. Similar to other evolutionary algorithms, this algorithm starts with an initial population. Each individual of the population is called a country. Some of the best countries (in optimization terminology, countries with the least cost) are selected to be the imperialist states and the rest form the colonies of these imperialists. All the colonies of initial countries are divided among the mentioned imperialists based on their power. The power of each country, the counterpart of fitness value in the GA, is inversely proportional to its cost.

The imperialist states together with their colonies form some empires. After forming initial empires, the colonies in each of them start moving toward their relevant imperialist country. This movement is a simple model of assimilation policy, which was pursued by some of the imperialist states. The total power of an empire depends on both the power of the imperialist country and the power of its colonies. This fact is modeled by defining the total power of an empire as the power of imperialist country plus a percentage of mean power of its colonies [16]. The steps of the proposed ICA are described as follows:

Step 1- Generate an initial colonies set with a size of N_c.
Step 2- Set iteration equal to 1.
Step 3- Calculate the objective function for each colony and set the power of each colony as follows:

$$CP_c = OF \tag{6}$$

Step 4- Keep the best N_{imp} colonies as the imperialists and set the power of each imperialist as follows:

$$IP_i = OF \tag{7}$$

Step 5- Assign the colonies to each imperialist according to the calculated IP_i. This means the number of colonies owned by each imperialist (Equation (8)), is proportional to its power, IP_i.

$$(IP_i / \sum_{j=1}^{N_{imp}} IP_j) \times (N_c - N_{imp}) \tag{8}$$

Step 6- Move the colonies towards their relevant imperialist using crossover and mutation operators.
Step 7- Exchange the position of a colony and imperialist if it is stronger $CP_c > IP_i$.
Step 8- Compute the empire's power, that is, EP_i for all empires as follows:

$$EP_i = \frac{1}{NE_i}\left(\chi_1 \times IP_i + \chi_2 \times \sum_{c \in E_i} CP_c\right) \tag{9}$$

where, χ_1 and χ_2 are weighting factors that are adaptively selected.
Step 9- Pick the weakest colony and give it to one of the best empires (select destination empire probabilistically based on its power, EP_i).
Step 10- Eliminate the empire that has no colony.
Step 11- If more than one empire remained then go to the sixth step.
Step 12- End [17].

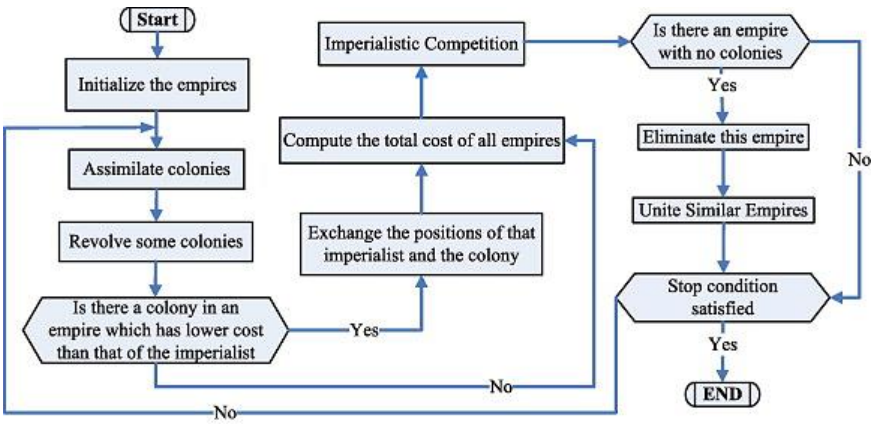


Figure 4. Flowchart of the Imperialist Competitive Algorithm

V. SIMULATION RESULTS

To validate computational results for switching angles, a simulation is done on Matlab/Simulink and m-file software for an 11-level cascaded H-bridge inverter with equal DC sources. ICA parameters are in Table 1. Simulation results are presented for modulation index M = 0.8 is shown in Table 2. The output phase voltage, line-line voltage waveforms, and frequency spectra of the line-line voltage are shown in Figures 5(a) to 5(d).

From the frequency spectra (FFT Analysis) of the output line voltage shown in Figure 5(d), it can be seen that the magnitudes of lower order 5th, 7th, 11th, and 13th harmonics are minimized. The THD result of the output line voltage shown in Figure 5(d), which is calculated according to the following, is 5.47%. Therefore, without the recalculation of optimum switching angles, the undesired harmonics (5th, 7th, 11th, and 13th in this case) will the *THD* of output voltage increases.

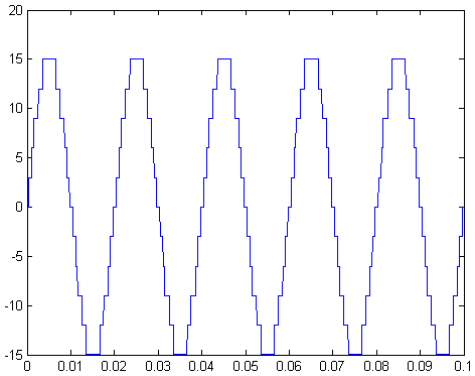
Table 1. ICA parameters

Number of countries	100
Max decades	150
Number of imperials	10

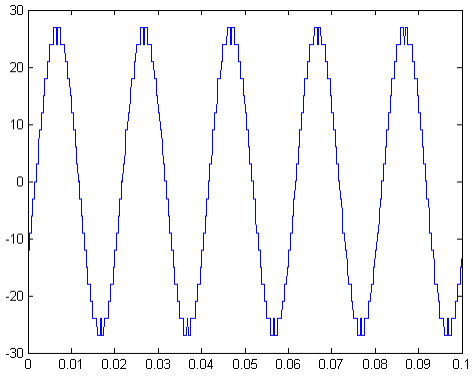
Table 2. Result of angles for 11-level cascade H-bridge inverter

M	θ_1	θ_2	θ_3	θ_4	θ_5
0.8	6.5772	18.9454	27.1891	45.1328	62.2385

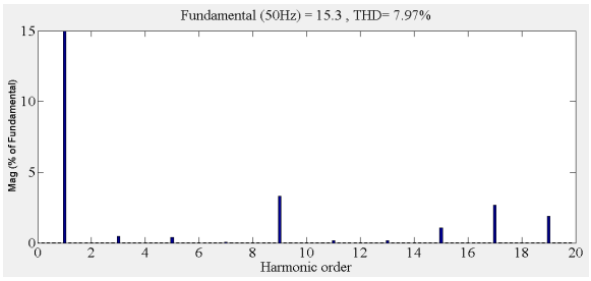
The proposed technique is applied to minimize defined cost function for the above stated case. The convergence characteristic of the ICA algorithm is depicted in Figure 6.



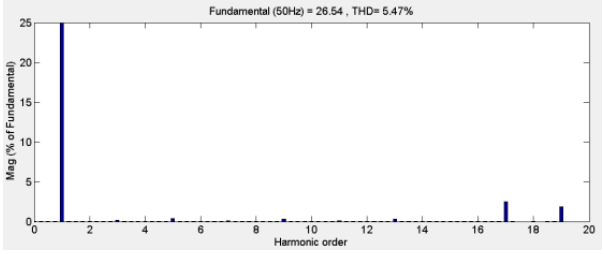
(a)



(b)



(c)



(d)

Figure 5. (a) Output phase voltage waveform, (b) Output line-line voltage, (c) FFT Analysis phase voltage, (d) FFT Analysis line voltage

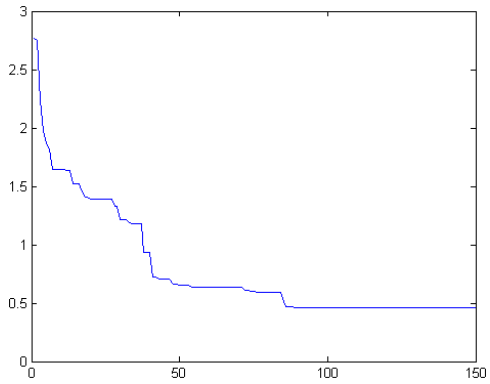


Figure 6. The Best Cost-Iteration diagram

VI. CONCLUSIONS

Different iterative methods are used to solve the nonlinear SHE equations such as Newton-Raphson. Since they have computationally expensive and the order of polynomials become very high for higher levels of multilevel inverter so optimization techniques are used to overcome these difficulties. In this paper, ICA has been proposed to solve SHE problem with equal DC sources in H-bridge cascaded multilevel inverter. The proposed method is able to find the optimum switching angles in a simple manner. They also reduce the computational burden and running time and ensure the accuracy and quality of the calculated angles. The simulation and experimental results are provided for an 11-level cascaded H-bridge inverter to validate the accuracy of the computational results.

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BIOGRAPHIES

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