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A NEW TOPOLOGY FOR MULTILEVEL INVERTER WITH REDUCED NUMBER OF COMPONENTS

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Abstract- In this paper, a novel structure for multilevel voltage source inverter is introduced, which can generate many levels. The number of required switches against required voltage levels is very important factors in designing of multilevel inverter, because switches define the cost, reliability, circuit size, installation area and control complexity. A comparison is made between proposed structure, the classical multilevel inverter structures, and other structures to reflect the merits of the presented structure. For proposed multilevel inverter, a novel algorithm for determination of voltage sources values are presented.

Keywords: Multilevel Inverter, Bidirectional Switch, Total Harmonic Distortion, Multi-Carrier PWM Method.

I. INTRODUCTION

The multilevel inverter structure has gained increasing attention in recent years particularly in applications involving medium and high voltage, such as static reactive power compensation and adjustable-speed drives [1-3]. A multilevel inverter is a power electronic device that synthesizes a desired output voltage from several levels of DC voltage sources as inputs. As the number of levels increase, the output voltage waveform becomes closer and closer to a sinusoidal waveform with fewer magnitude of harmonic content. Many kinds of structures of multilevel inverters have been proposed. In general, there are three types of multilevel inverters:

- Diode clamped [4]
- Flying-capacitor [5]
- Cascade [6]

Conventional cascade multilevel inverter is one of the most important structures in the family of multilevel inverters [7]. Cascade inverter requires the least number of components when compared to flying capacitor and diode clamped inverter [8]. The most important Part in multilevel inverters is switches, which increase the cost, control complexity, and tend to reduce the overall reliability and efficiency [9].

New structures with reduced number of switches and DC voltage sources have been presented in [10, 11]. However, these structures require to a large number of switches. Moreover, modulation techniques and control strategies have been developed for multilevel inverters such as sinusoidal PWM, selective harmonic elimination (SHE-PWM), and space vector PWM (SV-PWM), and others [12-13]. The most popular and simple high frequency switching scheme for multilevel inverter is multi-carrier PWM strategy [14-15]. This paper focuses on multi-carrier PWM modulation for trigger the power electronic switches for controlling the voltage levels generated on the output voltage.

In this paper, a new structure for multilevel inverter proposes to increase the number of levels with less number of switches and gate driver circuits. The comparisons among classical multilevel inverters and proposed structures in [10, 11] with new structure is presented. New methods are expressed for calculate the values of the required DC voltage sources in proposed structures. Additionally, in this paper multi-carrier PWM method is used for 7-level and 9-level multilevel inverters. Finally, simulation results verify the validity of the proposed multilevel inverter.

II. PROPOSED STRUCTURES IN [10] AND [11]

In [10], a new structure for multilevel inverter has been presented, which has reduced the number of switches. The basic unit of the sub-multilevel inverter, presented in [10], is illustrated in Figure 1(a). Figure 1(b) shows k basic units inverters connected in series, where the structure of the first till kth sub-multilevel inverter has n_1, n_2, ..., n_k bidirectional switches, respectively. The number of output voltage levels (N_{level}), IGBTs (N_{IGBTs}) and gate driver circuits (N_{driver}) are calculated using the following equations, respectively:

$$N_{level} = 2\left(n_1 \times n_2 \times n_3 \times \ldots \times n_k\right) - 1 \quad (1)$$

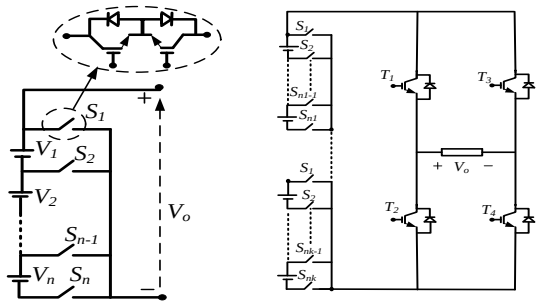
$$N_{IGBTs} = 2\left(n_1 + n_2 + n_3 + \ldots + n_k\right) + 4 \quad (2)$$

$$N_{driver} = \left(n_1 + n_2 + n_3 + \ldots + n_k\right) + 4 \quad (3)$$

In this structure, using the proposed optimal structure:

$$n_1 = n_2 = n_3 = \ldots = n \quad (4)$$

The maximum number of voltage levels for this topology is obtained for $n = 3$ and the minimum number of gate drive circuits to realize (N_{level}) values for voltage V_0 is realizable for $n = 2$. However, the main drawback of this structure is the utilization of a large numbers of bidirectional switches.



(a) (b)

Figure 1. (a) Basic unit in [10], (b) *K* basic units connected in series in [10]

To overcome aforementioned disadvantages, a new structure of multilevel inverter has been investigated in [11]. The structure of multilevel voltage source inverters, which is recommended in [11], is shown in Figure 2. This structure is capable to obtain all possible additive and subtractive combinations of the input DC levels in the load voltage. Though all such levels can be obtained using the proposed structure, the actual number of levels depends on the DC source arrangement.

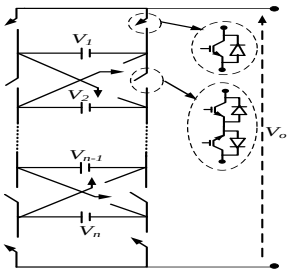


Figure 2. Suggested topology in [11]

For *n* DC voltage source, then the number of voltage levels count is:

- For unary method:

$$N_{level} = 2n+1 \quad \text{if} \quad V_{j-1} = V_j \quad , \quad j = 1,2,\ldots,n \tag{5}$$

- For binary method:

$$N_{level} = 2^{(n+1)} - 1 \quad \text{if} \quad V_{j-1} = 2V_j \quad , \quad j = 1,2,\ldots,n \tag{6}$$

- For trinary method:

$$N_{level} = 3^n \quad \text{if} \quad V_{j-1} = 3V_j \quad , \quad j = 1,2,\ldots,n \tag{7}$$

It is noticeable that the presented structure in [11] has been used bidirectional switches that has been composed of two IGBTs. Therefore, to compare the different structures, the numbers of IGBTs (instead of switches) are used in this paper. The number of IGBTs (N_{IGBTs}) and gate driver circuits (N_{driver}) are given by:

$$N_{IGBTs} = 6n - 2 \tag{8}$$

$$N_{driver} = 4n \tag{9}$$

However, the inverter needs a large numbers of IGBTs and gate driver circuits.

III. PROPOSED TOPOLOGY

The basic structure for proposed multilevel inverter is shown in Figure 3. This structure consists of a full-bridge converter and a basic unit. The basic unit consists of two DC voltage sources, two diodes and three IGBTs, which each one of IGBTs has an antiparallel diode.

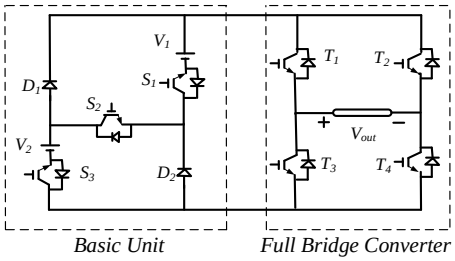


Figure 3. Suggested Basic structure for multilevel inverter

Table 1 shows the values of voltages V_{out} for different states of the switches S_1, S_2, ..., S_5, T_1, T_2, T_3 and T_4.

Table 1. Values of V_{out} for different states of the switches

	Switches							
State	S_1	S_2	S_3	T_1	T_2	T_3	T_4	V_{out}
1	0	0	0	1	1	0	0	0
2	1	0	0	1	0	0	1	V_1
3	1	0	0	0	1	1	0	$-V_1$
4	0	0	1	1	0	0	1	V_2
5	0	0	1	0	1	1	0	$-V_2$
6	1	1	1	1	0	0	1	(V_1+V_2)
7	1	1	1	0	1	1	0	$-(V_1+V_2)$

In this circuit, when the S_1, S_2 and S_3 switches are turned on, the D_1 and D_2 diodes are reverse biased and current flows from the V_1 and V_2 voltage sources. Note that there are different switching patterns for producing the zero level, and in Table 1, only one of them is shown. For instance, when the S_1, S_2, S_3, T_2 and T_3 switches are turned off, current flows from D_1 and D_2 diodes, anti-parallel diode of S_2 switch, T_1 and T_4 switches and output voltage is zero. The basic unit shown in Figure 3 can be extended as shown in Figure 4. The basic units in series can increase the possible values of V_{out}. For the proposed structure, three different methods for the determination of the values of the DC voltage sources are introduced.

A. First Proposed Method

In this method, all of the DC voltage sources are equal to *V*. In other word, we have:

$$V_1 = V_2 = \ldots = V_k = V \tag{10}$$

This structure is called symmetric multilevel inverter. The number of output voltage levels and maximum output voltage $V_{o,\max}$ can be determined by following equations:

$$N_{level} = 2k+1 \tag{11}$$

$$V_{o\max} = kV \tag{12}$$

B. Second Proposed Method

In the second method, the values of DC voltage sources to be chosen according to the following procedure:

$$V_1 = V \tag{13}$$

$$V_j = 2V \quad \text{for} \quad j = 2,3,4,\ldots,k \tag{14}$$

In this algorithm, the number of output voltage levels and maximum output voltage are obtained as follows:

$$N_{level} = 4k-1 \tag{15}$$

$$V_{o\max} = (2k-1)V \tag{16}$$

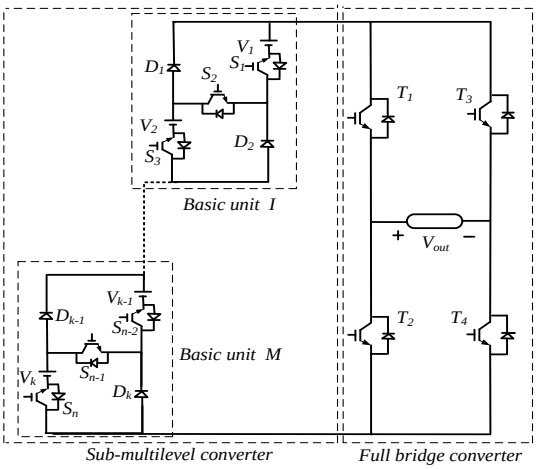


Figure 4. Suggested multilevel inverter

C. Third Proposed Method

In this method, the values of the DC voltage sources must be chosen using the following algorithm:

$$V_1 = V \tag{17}$$

$$V_j = 2^{(j-1)} V \quad \text{for} \quad j = 2,3,4,...,k \tag{18}$$

The number of output voltage levels and maximum output voltage are calculated by Equations (19) and (20), respectively:

$$N_{level} = 2^{(k+1)} - 1 \tag{19}$$

$$V_{o\max} = (2^k - 1)V \tag{20}$$

In this structure, number of IGBTs (N_{IGBTs}) is given by:

$$N_{\text{IGBTs}} = \frac{3k}{2} + 4 \tag{21}$$

It is noticeable that k is even number because each basic unit requires two DC voltage sources. It is important to note that the number of IGBTs and the gate driver circuits are the same.

IV. COMPARISON OF SUGGESTED TOPOLOGY WITH CLASSICAL MULTILEVEL TOPOLOGIES AND RECOMMENDED IN [10, 11]

The main purpose of this paper is reduction of the power electronic switches and gate driver circuits in comparison of the classical multilevel inverters and proposed structure in [10, 11].

A. Comparison of Proposed Structure with Classic Multilevel Inverters

The comparison between the classical multilevel inverter structures and suggested structure in terms of component requirements for a 7-level output voltage is listed in Table 2. It is evident that the power electronic components have been reduced significantly.

B. Comparison of Proposed Structure with Proposed Structures in [10, 11]

Figure 5 compares the number of IGBTs versus the number of output voltage levels in the third method of proposed structure, suggested structure in [10] and trinary configuration in [11]. This figure shows that the suggested topology needs fewer numbers of IGBTs.

Table 2. Comparison of classical structures and the proposed structure for seven level output

Output Voltage levels	Components	Classical multilevel inverter structures			Proposed topology
		Diode clamped	Flying capacitors	Cascaded	
7	IGBTs	12	12	12	7
7	DC bus capacitors	6	6	3	2
7	Clamping diodes	42	0	0	2
7	Clamping capacitors	0	15	0	0
7	Gate driver	12	12	12	7

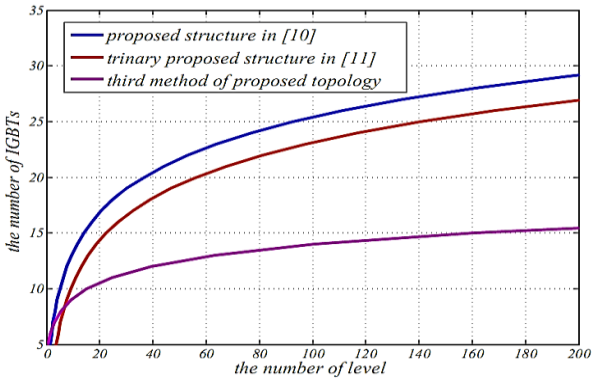


Figure 5. Comparison of the required number of IGBTs in the suggested structure and proposed structures in [10, 11]

Figure 6 shows the required number of gate driver circuits for realizing N_{level} of voltages for V_{out} in the third method of proposed topology, suggested topology in [10] and trinary configuration in [11]. This figure shows that the third method of proposed topology requires less number of gate driver circuits than [10, 11].

V. MULTI-CARRIER PWM STRATEGY

The harmonics in the output voltage of power electronic inverters can be reduced using PWM switching techniques [16]. The widely used multi-carrier PWM methods are known as Phase Shifted (PS), Phase Disposition (PD), Phase Opposition Disposition (POD), Alternative Phase Opposite Disposition (APOD), Hybrid (HD) and Phase Shift (PS) [17].

For this topology, phase disposition, (PD) multi-carrier PWM method is utilized. PD technique employs a number of carriers (m - 1) for an m-level phase waveform which are all in-phase accordingly [18]. The carriers are defined with the same frequency (f_c) and amplitude (A_c). The amplitude of the modulator is denoted as (A_m) and the frequency (f_m). In multilevel inverters, the amplitude modulation index (m_a), and the frequency ratio (m_f), are given by Equations (22) and (23), respectively:

$$m_a = A_m / (m-1) A_c \tag{22}$$

$$m_f = f_c / f_m \tag{23}$$

The switching functions of proposed multilevel inverter are given by the use of logical AND, OR, NOT gates.

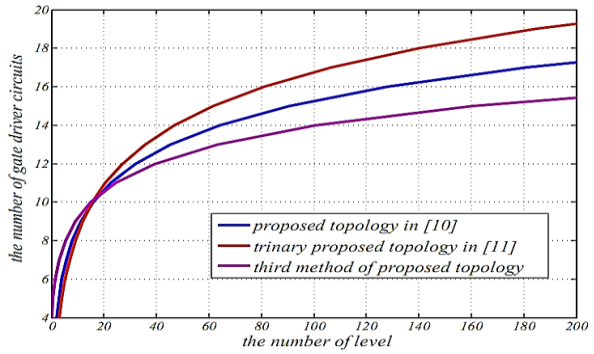


Figure 6. Comparison of the required number of gate driver circuits in the suggested structure and proposed in [10, 11]

VI. SIMULATION RESULTS

In order to validate the proposed multilevel inverter, MATLAB-Simulink software has been used. The total harmonic distortion (*THD*) evaluates the quantity of harmonic contents in the output waveform and is a popular performance index for power converters. The simulation studies are carried out for 7-level and 9-level multilevel inverters. The parameters selected for testing are: (a) An LC filter with L = 10 mH and C = 15 µf, and (b) a resistive load of 30 Ω, switching frequency of 1000 Hz. The simulation studies are carried out for two different cases.

A. Case 1 (Two DC Voltage Sources)

Since the value of two sources are selected with third method arrangement, number of levels will be $2^3 - 1 = 7$. Figure 7 shows the structure of proposed 7-level multilevel inverter.

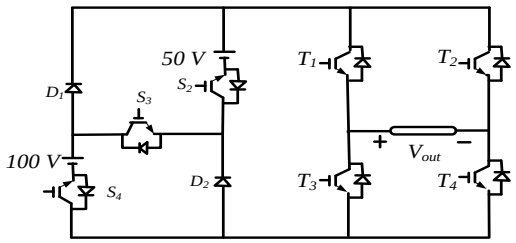


Figure 7. The 7-Level multilevel inverter (according to third method)

Figure 8 shows the carriers and reference signals for a 7-level PWM using PD technique with m_a = 1, m_f = 20. The output voltage and current waveforms and their corresponding Fourier spectrums are shown in Figures 9 and 10, respectively. *THD* of the output voltage and current based on simulations are equal with 24.36% and 18.52%, respectively. To generate a desired output with best quality of the waveform is used LC filter, which *THD* is shown in Figure 11 and is 8.51%.

B. Case 2 (Four DC Voltage Sources)

Figure 12 shows a configuration of the proposed inverter. Since the magnitude of four DC sources have been selected with the first method arrangement, the number of levels will be (2×4) + 1 = 9.

Table 3 shows the ON switches look-up table for 9-level inverter. Figure 13 shows the carriers and reference waveforms for 9-level multilevel inverter.

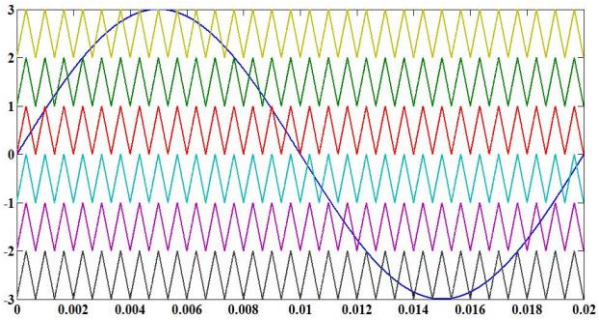


Figure 8. Reference and Carrier Signals for 7-level inverter

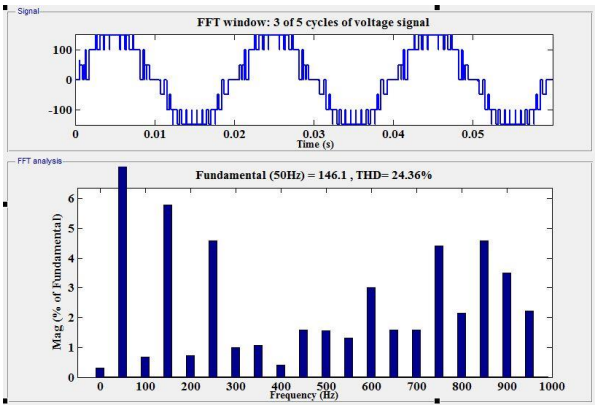


Figure 9. Output voltage and harmonic spectrum of 7-level inverter (*THD*=24.36%)

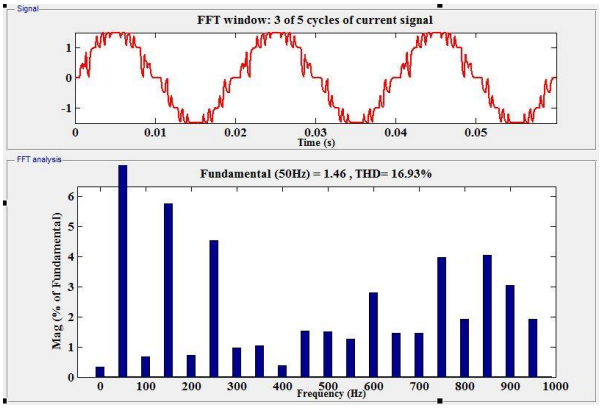


Figure 10. Output current and harmonic spectrum of 7-level inverter (*THD*=16.93%)

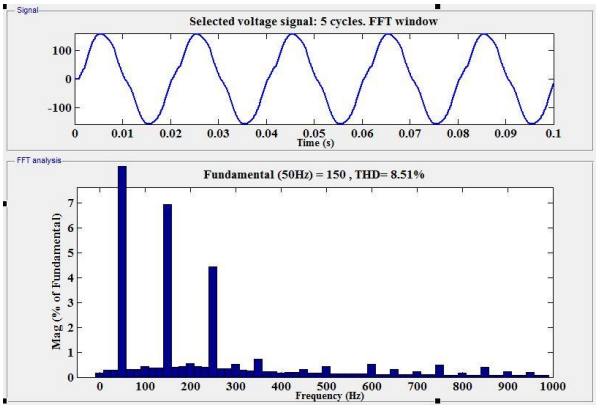


Figure 11. Output voltage and harmonic spectrum of 7-level inverter with LC filter (*THD*=8.51%)

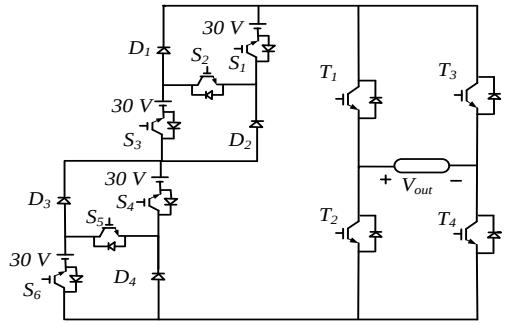


Figure 12. 9-Level multilevel inverter (according to first method)

Table 3. V_{out} values for different states of switches for 9-level inverter

	Switches States										
State	S_1	S_2	S_3	S_4	S_5	S_6	T_1	T_2	T_3	T_4	V_{out}
1	0	0	0	0	0	0	1	0	1	0	0
2	1	0	0	0	0	0	1	0	0	1	30
3	1	0	0	0	0	0	0	1	1	0	-30
4	1	1	1	0	0	0	1	0	0	1	60
5	1	1	1	0	0	0	0	1	1	0	-60
6	1	1	1	1	0	0	1	0	0	1	90
7	1	1	1	1	0	0	0	1	1	0	-90
8	1	1	1	1	1	1	1	0	0	1	120
9	1	1	1	1	1	1	0	1	1	0	-120

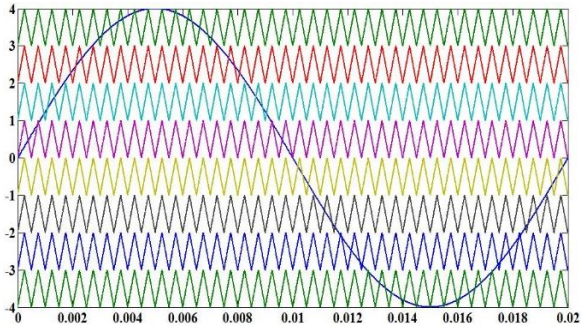


Figure 13. Triangular comparison with sine wave for 9-level inverter

The load voltage and current waveforms and their corresponding harmonic spectrums are shown in Figures 14 and 15, respectively. *THD* of the load voltage and current based on simulations are the same and is equal with 14.07%. For this case, *THD*s of the output voltage with LC filter based on simulation is 3.01%, shown in Figure 16.

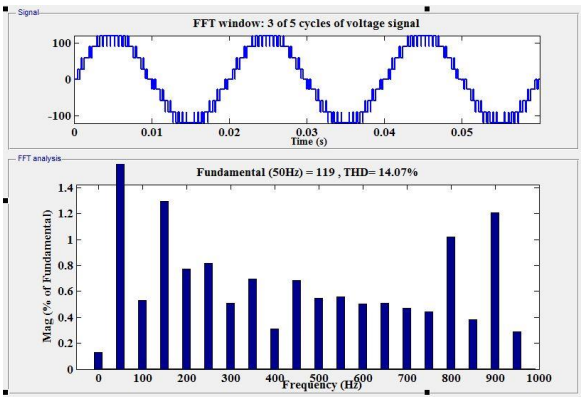


Figure 14. Output voltage and harmonic spectrum of 9-level inverter (*THD*=14.07%)

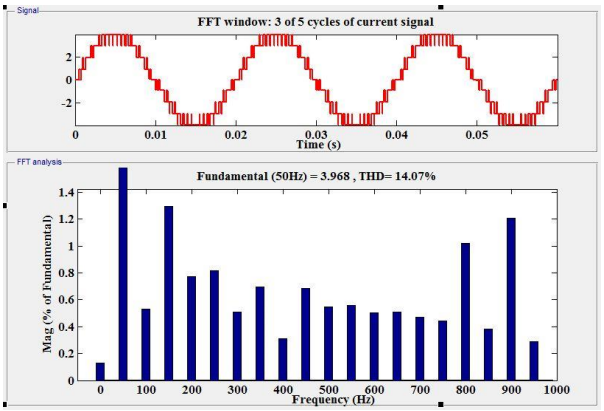


Figure 15. Output current and harmonic spectrum of 9-level inverter (*THD*=14.07%)

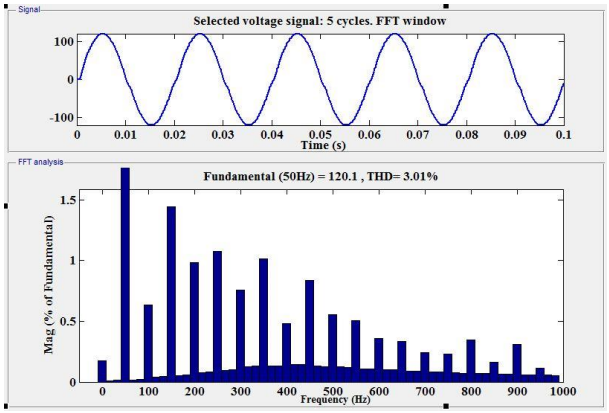


Figure 16. Output voltage and harmonic spectrum of 9-level inverter with LC filter (*THD*=3.01%)

VII. CONCLUSIONS

In this paper, a new structure for multilevel inverter with reduced number of power electronic switches and gate driver circuits was proposed. Three methods for determination of DC voltage source values were suggested. These techniques provide more voltage levels without increasing number of power electronic components.

Comparison among the proposed converter with classic topologies and other similar topologies was provided. It was shown that the proposed topology can produce many levels with fewer IGBTs. Multi-carrier PWM method was applied to the new topology to trigger the power switches for controlling the voltage levels generated on the output.

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BIOGRAPHIES

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