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MODELING OF STACKABLE EMBEDDED CAPACITORS INTO PCB LAYERS

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Abstract- In this paper the main characteristics and parameters of a stackable capacitor with variable capacitance embedded intro the PCB layers are presented. Embedding the passive components into the PCB will result into shorter trace distance for decoupling capacitors of MCU and IC resulting into an improvement of power integrity. The development of stackable embedded capacitors provides some alternative solution regarding the placement of capacitance in a PCB. The simulation of different topologies of capacitors and the modeling of the capacitors is done using FEM platform.

Keywords: Embedded Capacitor, Modeling, PCB Layers, Stackable Capacitance.

I. INTRODUCTION

Nowadays and in this context the meaning of the word "embedded" in general it refers to the techniques that are used to introduce extra amounts of capacitance into the raw PCB platform [1]. The most common way to do this is by deliberately spacing the power and ground planes together. Since the capacitance is inversely proportional to the distance between the planes. As an example if you build an 8-inch square, 6-layer FR-4 board with a pitch of 0.012 inches between the ground and power planes, you get an capacitance approximately equal to $226 \cdot \varepsilon_r \cdot Area$ in square inches.

Until now the only way to add a capacitance to a circuit board is done by attaching this capacitance to the PCB in two ways: trough hole or solder mounting it. At higher frequencies above 200 MHz the attachment of the external capacitor to the PCB may cause critical influences over the functionality of the system. The embedded capacitance has the potential to correct these issues and improve the adding of the extra capacitance that is needed. Used correctly the embedded capacitance provide a versatile solution for decoupling of the IC at frequencies above 400 MHz, especially when the distances between the power and ground plane is approximately 10 miles.

II. AN OVERVIEW AND CLASSIFICATION OF CAPACITORS AND MATERIALS

A. Capacitor Classification

Generally capacitors can be classified in tree types:

1. Electrostatic capacitors
2. Electrolytic capacitors
3. Electro-chemical capacitors

The electrostatic capacitors are constructed mainly from two metal "parallel plates" called electrodes, and they are separated by a dielectric as shown in Figure 1. The dielectric is a non-conducting material that is between electrodes. The operating voltage of the capacitor is proportional with the strength of the dielectric material that is used and it is measured in Volts per meter.

$$C = \frac{Q}{V} \tag{1}$$

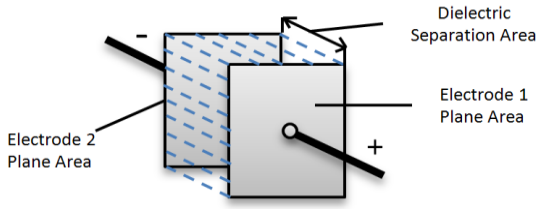

Figure 1. Representation of the capacitor with parallel plates and dielectric section

As an example the dielectric strength of the air is 3×10^6 [V/m], the diamond has 2×10^9 [V/m] and the paper 16×10^6 [V/m]. The value of dielectric parameter increases the overall value of capacitance and the maximum operating voltage in the capacitor. The capacitance is measured in Farads [F] and represents the ratio between the total charge in coulombs [Q] on each electrode and the value of the potential difference [V] between the pair of plates [1].

The Electrolytic capacitors share a similar pattern of construction to the electrostatic capacitor, but in this case it has substitute the conductive electrolyte with a salt based electrolyte which is placed in direct contact between the metal electrodes.

One of the common capacitor of this type is the aluminum electrolytic capacitor which is made from two aluminum conductive foils/plates which are coated with an insulating oxide layer and as a dielectric a paper soaked in electrolyte. The thin oxide layer ensures the dielectric functionality and also provides a higher capacity. This type of capacitors has a plus and minus polarity as a result of the oxide layer, which is spatial stabilized by the electric field established during the charge period. If the polarity of the capacitor is reversed-biased, the oxide thin layer is dissolved into the electrolyte and can become shorted and rarely in some cases it heats up and explode [2].

The Electro-chemical capacitors use a similar solution as the electrolyte but they have a greater capacitance per unit volume, due to their porous geometry of the electrode in comparison with the electrostatic and electrolytic capacitors.

$$C = \varepsilon_0 \varepsilon_r A / d \quad (2)$$

In Equation (2) is stated that by having a very large electrode surface-area (A) as a result of the porous electrodes and a very small separation gap (d), between the electronic and ionic charge at the electrode surface will result into a higher capacitance. The surface of the porous electrodes can be very large with values between $1000-2000$ [m^2/cm^3] [3]. The greater capacitance per unit volume of electro-chemical capacitors (EC) implies a high-energy density which is different from the energy density of conventional capacitors [4].

B. Embedded Capacitance into PCB

One of the main purposes of embedded capacitor is to perform decoupling function for the IC and other active components on the PCB. This function is critical because of the amount of current which is drawn by active components on the PCB. This can cause a transient voltage into the distribution power bus. This transient noise voltage may produce electromagnetic interferences (EMI) and can interfere with the normal functionality of the components placed on the board. The transient voltage also may induce currents on the I/O attached cables thus radiating the EMI. Other problem referees to the ground bounce or delta-I noise of the return plane, and in general this problem is common on the design of high-speed PCB and multichip module (MCM).

To solve these problems discrete decoupling capacitors are used, over the years decoupling capacitors have become smaller and smaller in dimension but also the number of chips on the board increased. Although they are smaller because of the huge number of them being needed on most of the chips they are occupying a large area on the board. Their effective frequency range is limited as a result of the interconnection inductance [5]. By increasing the number of decoupling capacitors on the PCB a reliability problem is imminent.

The embedded capacitance has lots of potential in solving all these issues as an alternative solution to the discrete decoupling capacitors [6]. Most of the PCB nowadays has more than 4 layers: Top layer, Power Layer, Ground (Return) layer and Bottom layer.

Embedding a capacitor into the PCB will use the distance between the Power and The Ground layer to provide power-bus decoupling. To enhance the capacitance, minimizing the spacing between the two solid planes must is mandatory. Also this space must be filled with a material that has a high permittivity characteristic.

C. Materials Used for Embedded Capacitors

Continuous development of dielectric materials which are commercially available is permanently renewed, as an example 3M Company released a 19-micron Embedded Capacitance Material (ECM), this type of material is thin and is used for embedded capacitor laminate on PCB. Material 3M C-PLY19 has a dielectric constant (DK) of 21 in comparison with FR-4 material which has approx. 4.0-4.5 and a capacitance density of 6.2 [nF/inch^2] [8]. This material helps in the reduction of the impedance and power bus noise, electromagnetic interferences and the count of the discrete capacitor [6].

The standard FR4 material used on the PCB boards combined with other more powerful dielectric materials can create a sustainable solution in adding of embedded capacitance to the PCB. Other solutions of materials involve a ceramic functional film embedded in the printed wiring board (PWB) using a build-up process. A key element to the low–cost board with embedded capacitors lays in the technology of ceramic deposition on the PCB substrates as FR4 material [7]. Other candidates are the polymer/ceramic composites, which are based on high dielectric constant of the ceramic powders and the perfect process compatibility of the polymers.

The Barrium Titanate $BaTiO_3$ is well-known ferroelectric material having a high dielectric constant [9]. This material are used in polymer/ceramic composites as ceramic filler for embedded capacitors. Also the multifunctional epoxy/$SrTiO_3$ composites materials can be used for embedded capacitors films.

III. MODELING OF EMBEDDED CAPACITORS

A. PDN Influences, Equivalent Schematic and PCB Traces

The stability of the Power Distribution Network (PDN) is critical in the PCB and decoupling capacitors on the core can mitigate the overshoot and self-resonance of the IC since it provides the PDN extra capacitance. High speed multilayered systems have an increase of the parasitic inductance in the PDN which affects the decoupling capacitors which are limited above some specific frequencies where the power impedance dramatically increase as a result of unexpected overshoot resonance [10]. In order to estimate the proper frequency range of the decoupling capacitors, the parasitic inductance and overshoot resonance must be calculated.

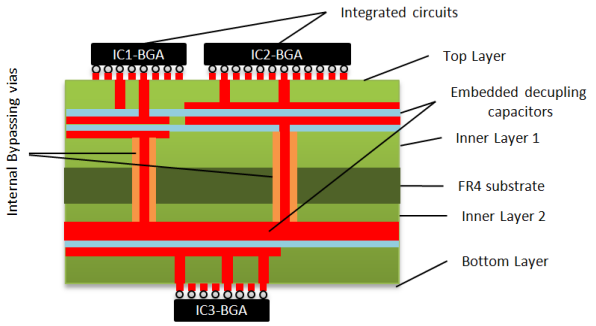

Figure 2. Schematic of discrete capacitors embedded into PCB layers

To properly analyze and simulate the power impedance characteristics of the PDN, the transmission line matrix (TLM) method must be used. The TLM method is used to successfully estimate the characteristics such as self and transfer impedance of the capacitors. The model of the embedded capacitor is the PCB is presented in the Figure 2, where the IC's are placed on the two sides of the board (Top and Bottom) and inner layers serve to Power and Ground planes.

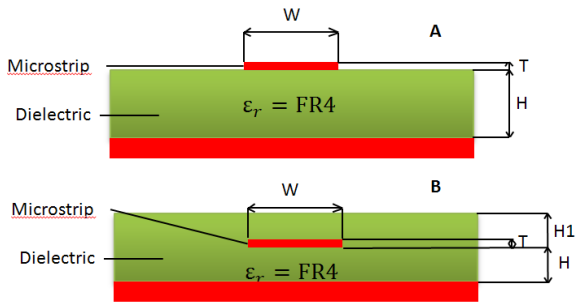

Figure 3. Types of microstrips used to model the trace impedance

The embedded decoupling capacitors are placed inside the PCB before and after the FR-4 substrate limit. Using the microstrip topology which is presented in Figure 3 calculation formula presented in Equations (3)-(9) we determine the trace impedance on the Top and Bottom layer.

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98H}{0.8W + T}\right) \text{ [}\Omega\text{]} \quad (3)$$

$$C_0 = \frac{0.67\left(\varepsilon_r + 1.41\right)}{\ln\left(\frac{5.98H}{0.8W + T}\right)} \text{ [pF/inch]} \quad (4)$$

$$T_{pd} = C_0 Z_0 \text{ [psec/inch]} \quad (5)$$

W=0.2, T=0.02, H=2, E_r=4.5 for Case A, Z_0=157 [Ω], $C0$=0.34 [pF/cm] and T_{dp}=53.4 [psec/cm] (3)-(5) and

$$Z_0 = \frac{87}{\sqrt{\varepsilon_r + 1.41}} \ln\left(\frac{5.98H}{0.8W + T}\right) \times \left(1 - \frac{H_1 - T - H}{0.1}\right) \text{ [}\Omega\text{]} \quad (6)$$

$$C_0 = \frac{T_{pd}}{Z_0} \text{ [pF/inch]} \quad (7)$$

$$T_{pd} = 84.75\sqrt{0.475\varepsilon_r \times \left(1 + e^{-1.55H_1/H}\right) + 0.67} \quad (8)$$

W=0.2, T=0.02, H=1.77, H_1=2.54, E_r=4.5 for Case B, Z_0=107.4 [Ω], C_0=0.518 [pF/cm] and T_{dp}=55.6 [psec/cm] (6)-(8), all dimensions are in [mm].

$$Z_0 = \sqrt{\frac{R + j\omega L}{G + j\omega C}} \quad (9)$$

$$C_e = C\left(1 + \frac{f^2}{f_0^2}\right) \quad (10)$$

All parameters of equivalent circuit schematics of a trance and a capacitor are presented in Figure 4: R_{ESR} (equivalent series resistance) involved into trace and connections is responsible for the heating of the component, E_{ESL} (equivalent series inductance) is highly dependent of the geometrical constraints of the component and R_{LEAK} (leakage resistance) depends of the dielectric type that is used. Conductance parameter for computational reasons is neglected and is considered approximately 0.

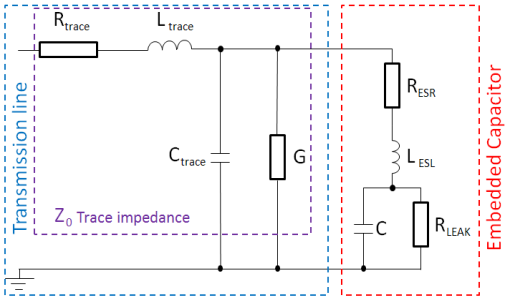

Figure 4. Equivalent circuit schematic of capacitor in a high speed system

The effective capacitance C is given by the Equation (10) with f operating frequency and f_0 resonance frequency is given by the Equation (11). The quality factor Q of the metal-insulator-metal (MIM) capacitor is given by the Equation (12)

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{1}{LC}} \quad (11)$$

$$Q = \frac{Q_c Q_d}{Q_c Q_d};\ Q_c = \frac{1}{wCR};\ Q_d = \frac{1}{\tan\delta} \quad (12)$$

The capacitor performance is associated with Q-factor and the parasitic inductance of capacitor [11].

B. Modeling embedded stackable capacitors

In this paper for the modeling and further experimental purposes the BC2000™ has been used with the fallowing dielectric composition FR4 epoxy/glass with a $\varepsilon_r = 3.8 \sim 4.2$ and a $\tan\delta = 0.015 - 0.02$. As model environment COMSOL Multiphysics™ has been selected and used.

Planar geometry has been used for low-costs reasons and simplification of the analysis and computational reasons. Stackable capacitors must have a repetitive pattern which can be easily reproduced in in fabrication operations.

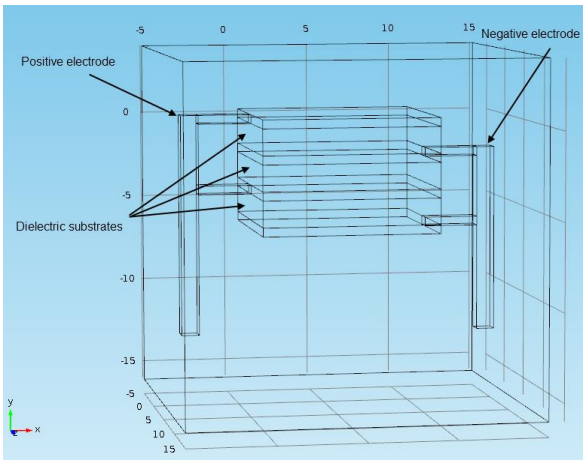

Figure 5. Geometrical model of the embedded stackable capacitor

The geometrical model and structure of the embedded capacitor can be seen in Figure 5. The distance between electrodes (d=the length of the dielectric fill), the area of the electrodes (positive and negative) is a square with *a*=length of one side and *t*=thickness of the electrodes, can be seen in the following Figure 6. The values are: *a*=10 [mm], *Area*=100 [mm^2], *d*=2 [mm], *t*=0.2 [mm].

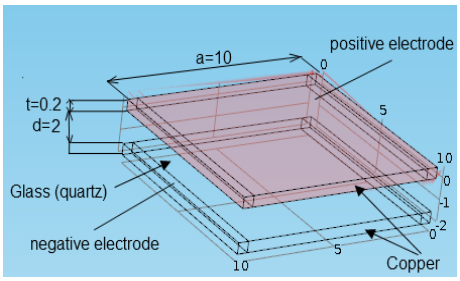

Figure 6. Dimensions of embedded stackable capacitor

The materials used for this model are: for all plates (positive and negative) Cu, for dielectric the materials used were glass (quartz) and FR-4. Using finite element method (FEM) we have made mesh for the capacitor, the mesh consists of 103818 domain elements, 9642 boundary elements, and 1168 edge elements and is presented in Figure 7.

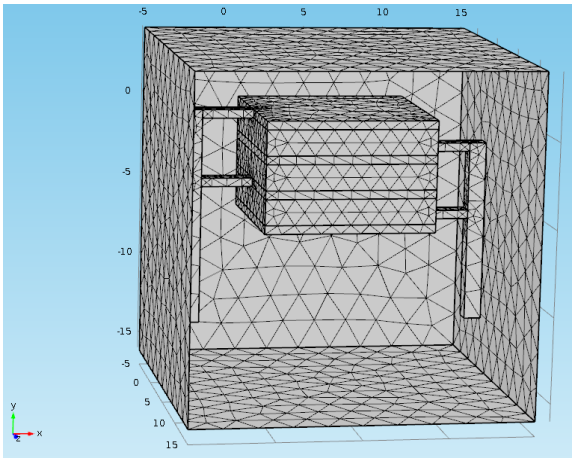

Figure 7. Model meshing of the embedded capacitor

High resolution approximation around edges and electrodes connections with parallel plates was required for better and accurate results.

IV. MODELING RESULTS

Electric potential field is a key element in this analysis. As it is known as the electric potential (*V*) in any point in the electric field is the electric potential energy (*U*) per unit charge associated with a test charge (*q'*) at that point (*V*=*U*/*q'*). As the capacitance is represented by the ratio of the magnitude of charge (*Q*) on either conductor to the magnitude of the potential difference (*V*) between the conductors (*l*). The electric field (*E*) is an important factor in modeling the capacitor. The analysis of electrical field on edges for plate capacitors (MIM) and other geometries of the electrodes are mandatory. The key areas of edges are marked in both figures. The target is to obtain a perpendicular field on electrodes surfaces.

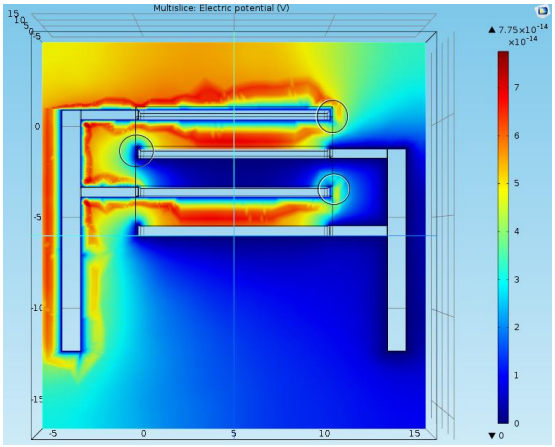

Figure 8. Electric potential modeling results for 7 [V]

The modeling results are presented in plot form in which the electric potential of the capacitor for 7 [V] terminal potential is presented in Figure 8 and for 12 [V] potential is presented in Figure 9.

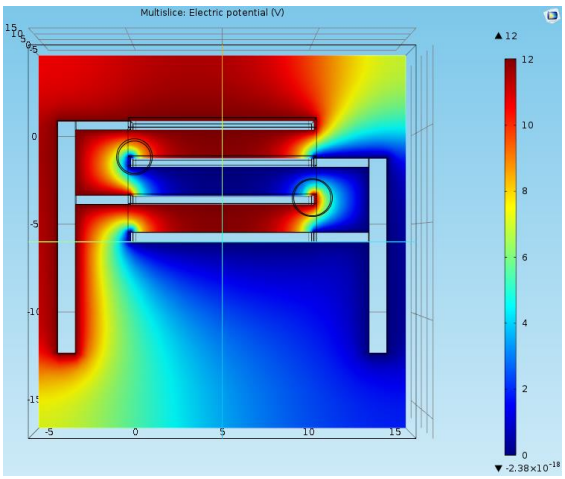

Figure 9. Plot of electric potential modeling results for 12 [V]

The capacitance obtained for different measurements and variation of dielectric material are: 1.1530E-11; 2.5876E-11; 2.4669E-11; 2.4440E-11; [F].

V. CONCLUSIONS

In order to create a viable embedded stackable capacitor into the PCB board, dielectric capabilities, geometrical characteristics on electrodes and constrains are critical. High-*k* dielectrics are good for small distance plate electrodes, providing high energy storage and high capacitance. To ensure proper usage of the capacitors for specific purposes, frequency analysis must be made to avoid resonance problems of IC and other devices. High frequency systems add line impedance and also EMI interferences. The stackable attribute of the capacitor is done by using simple geometries of the electrodes, avoiding complex forms that may raise problems on repetitive pattern of the manufacturing process. Modeling and simulations provide low cost good quality analysis and tuning of the embedded capacitors providing useful information about characteristic and parameters of the capacitor.

Simple geometries provide low-cost fabrication. For further research 3D printers can be used in order to manufacture custom boards with embedded capacitors, for decoupling functions or signal filtering.

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BIOGRAPHY

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