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# SWITCHED INDUCTOR CAPACITOR BASED DC-AC CONVERTER FOR PV APPLICATIONS

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**Abstract-** A two stage DC-AC converter topology which features a Switched Inductor Capacitor (SLCN) DC-DC converter and a single-phase H-bridge inverter is proposed by this paper. The SLCN converter has 11 passive components, one voltage source and one power switch, the H-bridge is composed of 4 power switches (IGBTs with antiparallel diodes). The main advantages of the proposed converter are high boost ratio, one power switch and reduced voltage stress across the switch on the DC-DC side, low component count, and it's implemented using simple control techniques. Also, the proposed topology is suitable for DC loads such electric vehicles, offers high voltage gain when compared to single stage converters. The proposed converter is suitable for PV applications because of the high voltage gain characteristics. Detailed analysis of the DC-DC section of the converter is analyzed in CCM, a theoretical gain of 20 at 80% duty cycle is achieved in steady state. The working principles of the proposed topology are validated by PSCAD simulations using 20 kHz switching frequency and 80% duty cycle for the DC-DC side and sinusoidal PWM technique for the DC-AC side.

**Keywords:** DC-DC Converter, H-Bridge Inverter, High Voltage Gain, Sinusoidal PWM, Switched Inductor Capacitor Network.

## 1. INTRODUCTION

Solar PV systems come in four different configurations namely, stand-alone (off grid), grid-tie (grid connected), grid-tie with backup (grid-interactive), and grid fall back. Grid fall back is a system that allows use of the solar PV array to charge a battery system, then power a house or part of the house until the batteries go flat, then the load falls back to the grid while the batteries recharge. A lot of solar PV installations come with a high initial cost and the consumer is required to install a system that meets grid requirements and other standards set by the utility company from the onset. Whereas, a grid fallback system allows the consumer to start with one panel and a 12 V battery.

To achieve a 240 V or higher dc or ac voltage from a grid fall back solar PV system, a boost ratio of 20 is required. Over the last few years, there has been increased interest in DC-DC converters to boost voltage for solar PV systems to meet the voltage level of most dc or ac loads. A number of step-up converters have been developed with various boost ratios, component quantities, and voltage stress across power devices and other circuit elements. Conventional boost converters are the simplest in control and structure, and they can attain high boost ratios but only on extreme duty cycles. However, at duty cycles above 90% there are significant issues like increased losses, EMI, and reverse recovery issues of the diode [1] in boost converters. As a result, some authors have explored the option to increase boost ratio in boost converters by using transformers. However, transformers are bulky and these converters require high frequency transformers which are costly [8]. Another drawback for converters with transformers is, the power devices experience high voltage spikes due to leakage inductance [11]. Z-source DC-DC converters can attain the 20-boost ratio with duty cycle less than 50%, but they have discontinuous input current, high voltage stress across the capacitor, have a different ground for input and output voltages, and they are not suitable for very low input voltages [5]. A quasi Z-source improves on some of the drawbacks on Z-source converters, but they still experience high stress on capacitor C1 and it's not suitable for very low input voltages [5] as well. Other dc-dc converters developed from the Z-source use more components than the original Z-source converter [5].

Switched inductor (SL) and switched capacitor (SC) based dc-dc converters have been developed to achieve higher voltage boost ratios. A SL structure is proposed by [3] which was derived from a Cuk dc-dc converter to achieve a high boost without increasing the duty cycle, by replacing the inductor in a conventional Cuk converter with a SL cell. At a 47% duty cycle, a 30 V DC input voltage fed into a [3] converter topology is regulated to 180 V DC at the output. However, it is not the required gain, and SL structures have an internal problem of high voltage stress on switches, because inductors are capable of unbalancing the current in a switching leg during a switching operation due to their behavior of being like current sources connected in series. To achieve higher voltage gains, [4] conducted an experiment which implemented a passive version with three SC cells, a nominal input voltage of 40 V DC at 47% duty cycle, an output voltage of 300 V DC.

Switched capacitor topologies are suitable for higher voltage gains but their component count tends to increase where higher boost ratio is required [11]. Additionally, the elements in a SC topology experience considerable current stress for higher voltage levels [19] and [20].

As a result, topologies which combine switched inductor and switched capacitor networks achieve very high boost ratios with moderate trade-offs on voltage stress (due to the effect of capacitors) and component count (due to the role of inductors in voltage boost). Therefore, to overcome the limitations related to extreme duty cycle, low input voltages, voltage stress across switches, and increase of components to achieve high boost ratios, a switched inductor capacitor network (SLCN) based dc-dc converter is used as a step-up dc-dc converter.

The proposed topology is a two stage DC-AC converter which has a DC-DC combined with a DC-AC topology. A 12V battery is used as input for the DC-DC topology and its output is the input of the DC-AC converter. The DC-DC topology is a switched inductor capacitor network (SLCN), and the DC-AC converter is a single-phase H-bridge inverter. The DC-DC topology has 5 diodes, 4 capacitors, 2 inductors, and a power electronic switch. It has a voltage gain of 20 at 80% duty cycle. The operating modes and their corresponding mathematical analysis of the DC-DC topology are investigated in this paper. The H-bridge has four power electronic switches which are controlled using sinusoidal PWM technique. The performance of the DC-DC and the DC-AC converters is validated by a simulation using PSCAD.

This paper is divided into four sections. Section II shows the mathematical analysis of the DC-DC and DC-AC sections of the proposed converter and also discusses their respective operating modes. Section III validates the theoretical analysis in section II by presenting simulation results generated from PSCAD. Finally, section IV gives concluding remarks on the investigation carried out.

## 2. NONLINEAR MOTOR DYNAMICS

Figure 1 illustrates the power circuit of the proposed two stage DC-AC converter. The operating modes and mathematical analysis of SLCN DC-DC converter and the H-bridge inverter are discussed in separate sub-sections.

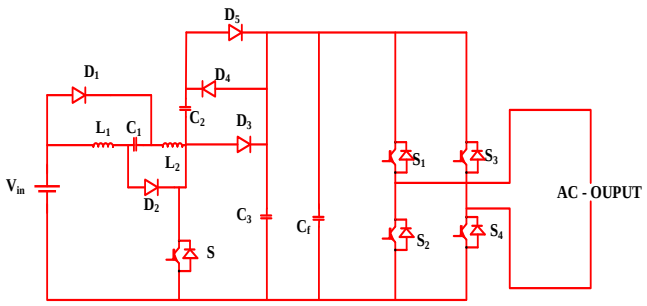


Figure 1. Proposed two stage DC-AC converter topology

### 2.1. SLCN DC-DC Converter Mode 1 Operation

The SLCN topology has two operating modes. Figure 2 shows the power circuit of the proposed topology in mode 1 operation; this state is initiated by closing switch S (switching on).

This results in reverse biased state of diodes $D_3$ and $D_5$ while diodes $D_1$, $D_2$, and $D_4$ are forward biased. Inductors $L_1$ and $L_2$, and capacitor $C_1$ are connected in parallel and are charged from the source voltage. When fully charged, the voltage across these components ($L_1$, $L_2$, $C_1$) equals to the source voltage, this represented by Equation (1). The inductor currents rise from minimum values to maximum values during this operating mode. Capacitor $C_3$ has a double boosted voltage and it charges capacitor $C_2$ through diode $D_4$. As a result, capacitor $C_2$ also has double boosted voltage as illustrated by equations (3). The current of the four passive elements being charged during this operation flows through the switch. First mode of operation ends when the switch opens. The filter capacitor $C_f$ delivers energy to the output side in this mode. The equations related to mode 1 are shown from Equations (1) to (7), and the corresponding analytical waveforms for mode 1 are shown in Figure 4 from $t_0$ to $t_1$.

$$V_{L1} = V_{L2} = V_{C2} = V_S \tag{1}$$

Using KVL in the loop that contains input source and capacitor $C_3$:

$$\begin{cases} -V_S + V_{L1} - V_{C1} + V_{L2} - V_{C2} + V_{C3} = 0 \\ V_{L2} = V_S - V_{L1} + V_{C1} + V_{C2} - V_{C3} \end{cases} \tag{2}$$

Using KVL in the loop that contains $C_f$ and $C_3$:

$$\begin{cases} -V_{C2} + V_{C3} = 0 \\ V_{C2} = V_{C3} \end{cases} \tag{3}$$

Using KVL in the loop with $C_f$ and load:

$$\begin{cases} -V_{Cf} + V_0 = 0 \\ V_0 = V_{Cf} \end{cases} \tag{4}$$

Substituting Equation (3) into Equation (2):

$$V_{L2} = V_S - V_{L1} + V_{C1} \tag{5}$$

And the relationship between currents is expressed as:

$$i_S = i_{L1} + i_{L2} + i_{C1} \tag{6}$$

$$i_{C2} = i_{C3} \tag{7}$$

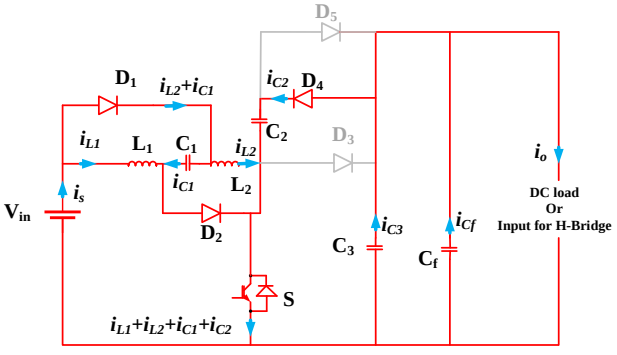


Figure 2. SLCN DC-DC converter in mode 1

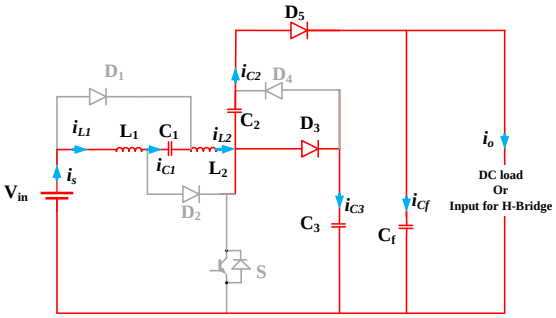


Figure 3. SLCN DC-DC converter in mode 2

### 2.2. SLCN DC-DC Converter Mode 2 Operation

The second operating mode is initiated when switch $S$ is opened (switching off). The equivalent circuit of the converter during this operation is shown by Figure 3. Diodes $D_1$, $D_2$, and $D_4$ are in off state, while diodes $D_3$ and $D_5$ are conducting mode. During this operating mode, inductors $L_1$ and $L_2$, capacitors $C_1$ and $C_2$, and the input deliver energy to the load. Simultaneously, the source, inductors $L_1$ and $L_2$, and capacitor $C_1$ discharges power to capacitor $C_3$. Capacitor $C_3$ acquires double boosted voltage across its terminals as shown by Equation (21). Inductor currents begin to decrease from maximum values to non-zero minimum values, and the energy stored in the inductors' magnetic fields falls. The current through capacitor $C_1$, and inductors $L_1$ and $L_2$ equals to the input current. Equations (8) to (11) show voltage and current relations, and analytical waveforms for mode 2 operations are shown by Figure 4 from $t_1$ to $T_S$. Note that the inductor voltage expression during this mode shown in Figure 4 is given by Equation (11).

Using KVL in the loop containing input source and $C_3$:

$$\begin{cases} -V_S + V_{L1} - V_{C1} + V_{L2} + V_{C3} = 0 \\ V_{L1} = V_S - V_{L2} + V_{C1} - V_{C3} \end{cases} \quad (8)$$

Using KVL in the loop containing $C_2$, $C_3$, and $C_f$:

$$\begin{cases} -V_{C3} - V_{C2} + V_{Cf} = 0 \\ V_{Cf} = V_{C2} + V_{C3} \end{cases} \quad (9)$$

Using KVL in the loop containing $C_f$ and load, $V_{cf}$ relates with $V_0$ as illustrated by Equation (4). And using KVL in the loop containing the input source and $C_f$:

$$\begin{cases} -V_S + V_{L1} - V_{C1} + V_{L2} - V_{C2} + V_{Cf} = 0 \\ V_{L2} = V_S - V_{L1} + V_{C1} + V_{C2} - V_{Cf} \end{cases} \quad (10)$$

$$V_{L1} = V_{L2} = \frac{V_0 - 4V_S}{4} \quad (11)$$

Definitions of switching period $T_S$

$$T_S = \frac{1}{f_S} \quad (12)$$

$$T_S = T_{ON} + T_{OFF} \quad (13)$$

And the duty cycle is defined as:

$$D = \frac{T_{\text{ON}}}{T_{\text{OFF}}} \quad (14)$$

Time when the switch is closed (switched on) is defined as;

$$T_{ON} = DT_S \quad (15)$$

And when the switch is open (switched off);

$$T_{OFF} = T_S - T_{ON} = T_S - DT_S = (1-D)T_S \quad (16)$$

Using the voltage balance law of the inductor, the average voltage of inductor 1 and 2 in one switching period is zero. Additionally, since the inductor values are the same, the voltage across inductor $L_1$ and $L_2$ are also equal.

$$V_{L1} = V_{L2} = V_L \quad (17)$$

$$(V_L)_{ON} + (V_L)_{OFF} = 0 \quad (18)$$

Using Equations (2) and (3):

$$\begin{cases} V_{L2} = V_S - V_{L1} + V_{C1} + V_{C2} - V_{C3} \\ 2V_L = V_S + V_{C1} + V_{C2} - V_{C3} \\ (V_L)_{ON} = \frac{1}{2}(V_S - V_{L1} + V_{C1} + V_{C2} - V_{C3})(DT_S) \end{cases} \quad (19)$$

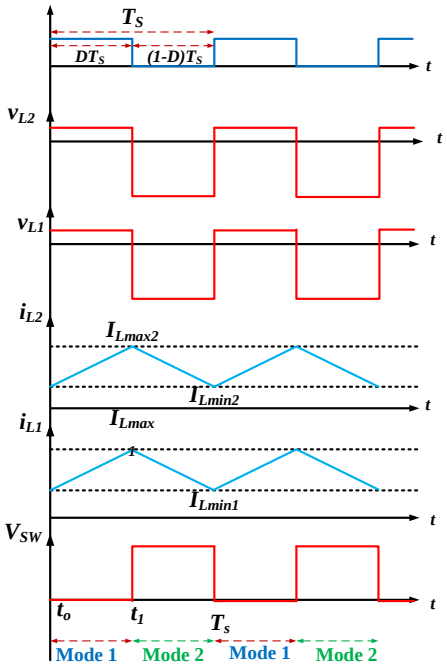


Figure 4. Analytical Waveforms for the SLCN Converter

Using Equation (8):

$$\begin{cases} V_{L1} = V_S + V_{C1} - V_{L2} - V_{C3} \\ 2V_L = V_S + V_{C1} - V_{C3} \\ V_L = \frac{1}{2}(V_S + V_{C1} - V_{C3}) \\ (V_L)_{OFF} = \frac{1}{2}(V_S + V_{C1} - V_{C3})(DT_S) \end{cases} \quad (20)$$

Using Equation (18):

$$\begin{cases} (V_L)_{ON} = -(V_L)_{OFF} \\ \frac{1}{2}(V_S + V_{C1} + V_{C2} - V_{C3})(DT_S) = \\ = \frac{1}{2}(V_S + V_{C1} - V_{C3})(1-D)T_S \\ V_{C2}D = -V_S - V_{C1} + V_{C3} \end{cases} \quad (21)$$

Substituting Equation (3):

$$\begin{cases} V_{C3}(D-1) = -1(V_S + V_{C1}) \\ V_{C3} = \dfrac{V_S + V_{C1}}{(1-D)} \end{cases} \quad (22)$$

Substituting Equation (1):

$$V_{C3} = \frac{2V_S}{1-D} \quad (23)$$

Substituting Equations (3) and (9) into Equation (4):

$$\begin{cases} V_{Cf} = V_{C2} + V_{C3} \\ V_{Cf} = 2V_{C3} \\ V_0 = V_{Cf} = 2V_{C3} \end{cases} \quad (24)$$

Substituting Equation (23) into Equation (24);

$$V_0 = 2\left(\frac{2}{1-D}\right)V_S \quad (25)$$

Therefore, the output voltage and the static gain ratio are expressed by;

$$V_0 = \frac{4}{1-D}V_S \quad (26)$$

$$G = \frac{V_0}{V_S} = \frac{4}{1-D}V_S \quad (27)$$

### 2.3. H-Bridge Inverter

Table 1. Different operating modes in an H-bridge inverter

| Operation Modes | Switch States | | | | Results |
|---|---|---|---|---|---|
| | $S_1$ | $S_2$ | $S_3$ | $S_4$ | |
| 1 | 0 | 1 | 0 | 1 | 0 V |
| 2 | 0 | 1 | 1 | 0 | $-V_{in}$ |
| 3 | 1 | 0 | 0 | 1 | $V_{in}$ |
| 4 | 1 | 0 | 1 | 0 | 0 V |

The number of operating modes in an H-bridge inverter are 16. However, only four are acceptable. The unacceptable switching modes cause short-circuit faults of the switches and open circuit fault of the load. Table 1 shows the acceptable switching modes. In operating mode 1 and 4, the output voltage is zero as shown in equation (28). In operating mode 2 and 3, the output voltage is negative or positive source voltage respectively; also illustrated by equation (28). The H-bridge inverter is controlled using sinusoidal PWM which compares the carrier signal ($V_c$) and the reference signal ($V_r$). Additionally, gate signals of switches $S_1$, $S_2$, $S_3$ and $S_4$ are also designed to follow the inequalities shown in Equations (30)-(33). Using KVL in the equivalent H-bridge circuit;

$$\begin{cases} V_0 = 0 \text{ V} \\ V_0 = V_{in} \\ V_0 = -V_{in} \end{cases} \quad (28)$$

$$\begin{cases} V_r < V_c \text{ and } -V_r > -V_c \\ V_r > V_c \\ -V_r < -V_c \end{cases} \quad (29)$$

The gates signals are also generated when the following inequalities are satisfied;

$S_1$ is ON when $V_c > V_r$ (30)

$S_2$ is ON when $V_r > V_c$ (31)

$S_3$ is ON when $V_r < 0$ (32)

$S_4$ is ON when $V_r > 0$ (33)

## 3. SIMULATION RESULTS

PSCAD simulation was carried out to validate the theoretical performance of the proposed DC-AC converter discussed in the previous section. Simulation variables for the DC-DC side and DC-AC sides of the converter are given in Table 2.

Simulation plots generated in PSCAD are shown by Figure 5 to 9. An arbitrary selection of simulation results for output voltage and current, passive elements voltages and currents, and switch currents and voltage for the DC-DC converter is presented in Table 3, with simulation results for the DC-AC converter side.

The DC-DC converter side has excellent boost capabilities as shown in Table 3 using three different input voltages in simulations. In all three cases the output voltage gain was approximately 20 at 80% duty cycle. The output voltage gain generated is slightly lower because of the effect of unwanted electrical properties in the components e.g., the switch resistance. The voltage across capacitors $C_2$ and $C_3$ are equal and are double boosted.

The switch voltage is approximately equal to half of the output voltage in all the three cases with different input voltages. Voltage stress is reduced across the switch in contrast to the boost converter where it is the same with output voltage. On the DC-AC converter side, the inverter successfully converts the 240V dc to 240V ac peak voltage. A performance comparison between different SLCN DC-DC converters based on boost ratio, voltage stress, and component count is also shown in Table 4.

Table 2. Simulation parameters for the proposed converter

| DC-DC CONVERTER SIMULATION PARAMETERS | |
|---|---|
| Input voltage, *Vs* | 12 V DC |
| Capacitors $C_1$, $C_2$, $C_3$, $C_f$ | 470 µF |
| Inductors $L_1$, $L_2$ | 3.3 mH |
| Load, *R* | 1000 Ω |
| Duty Cycle, *D* | 80% |
| Switching frequency, *fs* | 20 kHz |
| Target output voltage, $V_0$ DC | 240 V DC |
| Switch type | IGBT with anti-parallel diode |
| DC-AC CONVERTER SIMULATION PARAMETERS | |
| Input voltage, Vin | 240 V DC |
| Load inductor, *L* | 10 mH |
| Load resistor, *R* | 2 Ω |
| Amplitude modulation index, $M_a$ | 0.7 |
| Carrier frequency, $f_c$ | 700 Hz |
| Target output peak voltage, $V_0$ AC | 240 V AC |
| Switch type | IGBT with anti-parallel diode |

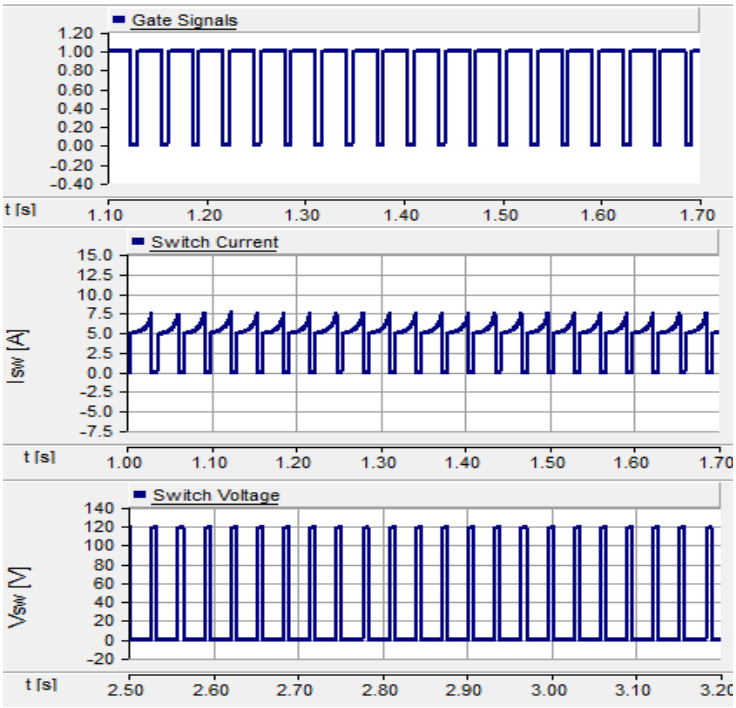


Figure 5. DC-DC converter switch characteristics for 12 V DC input

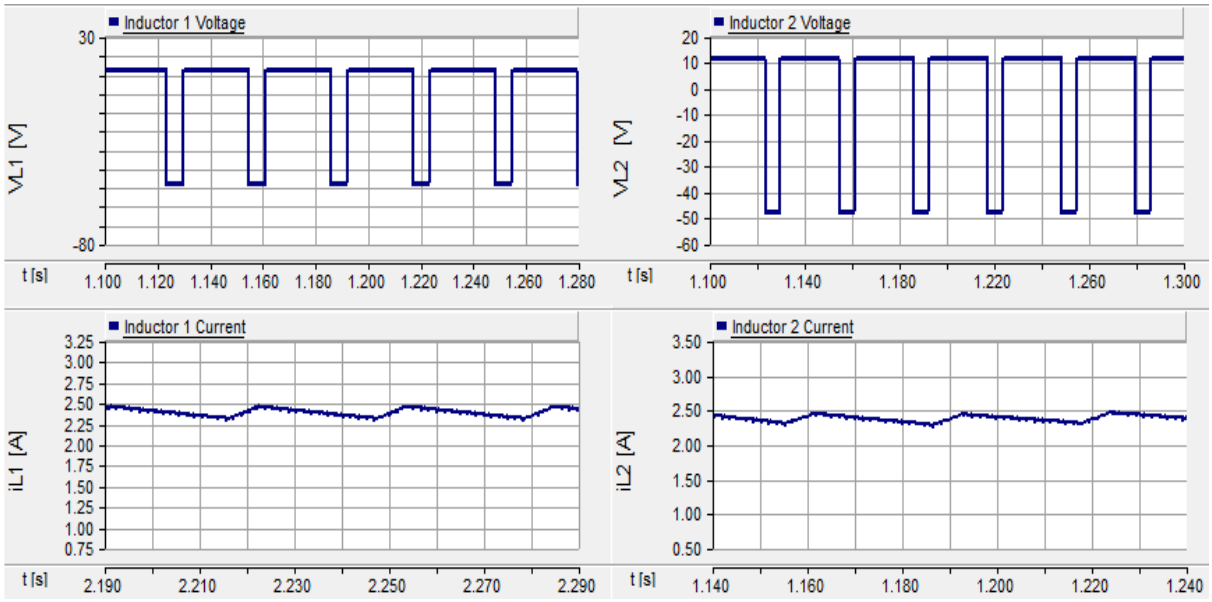


Figure 6. Inductors 1 and 2 voltage and current for 12 V DC input

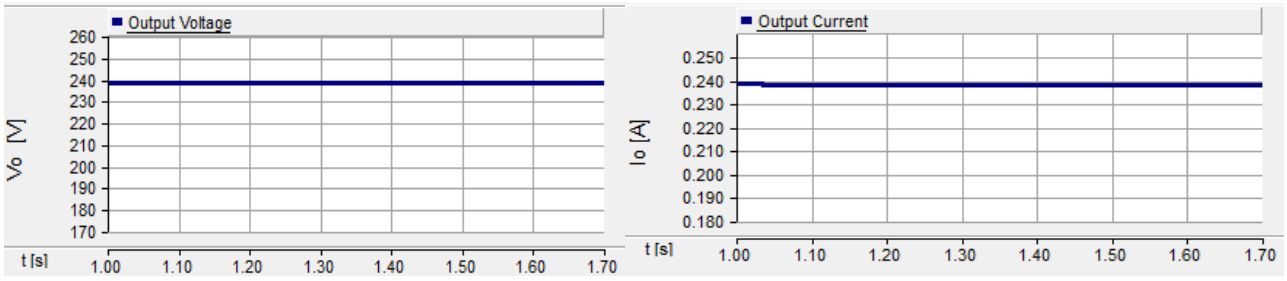


Figure 7. DC-DC topology voltage and current output waveform

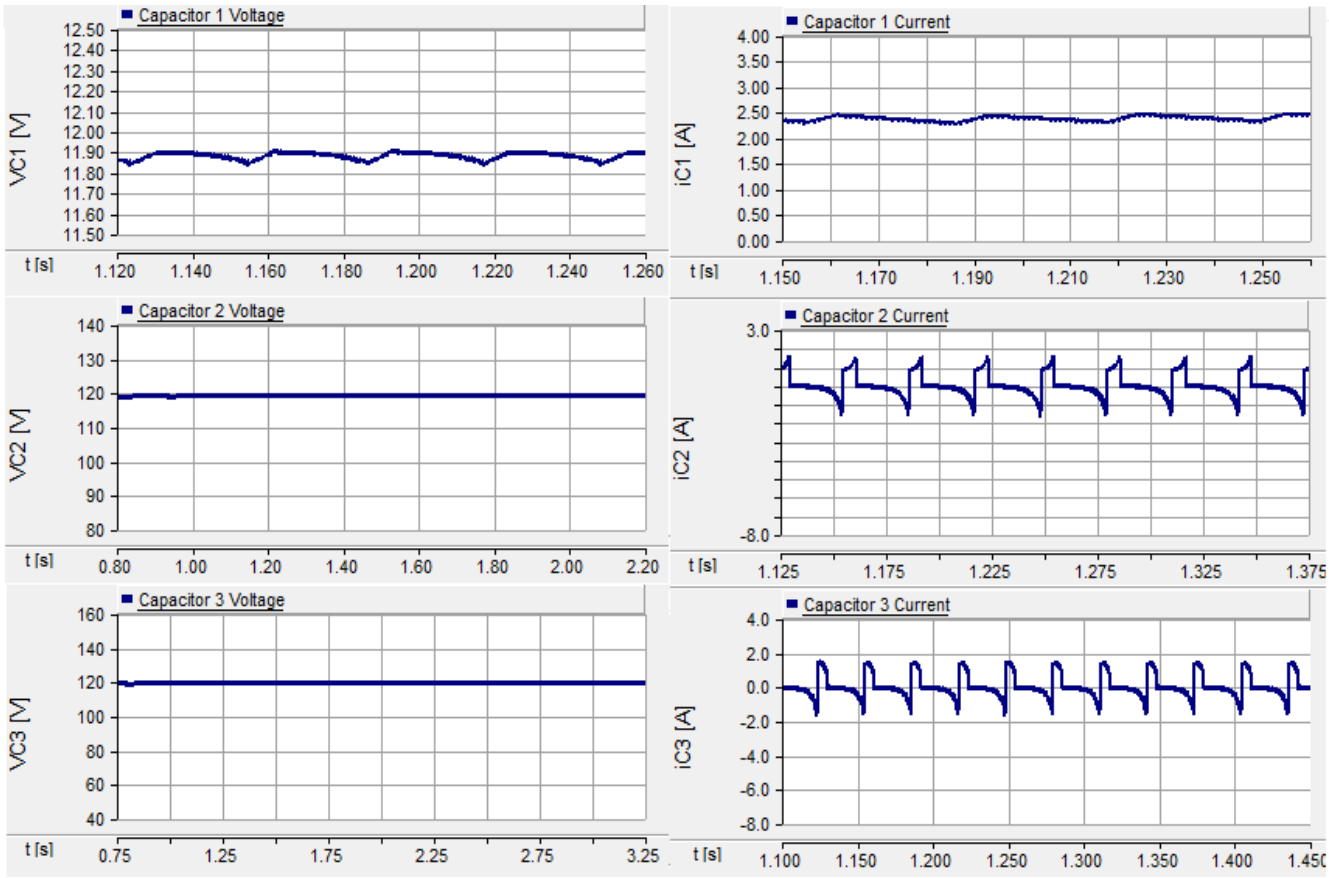


Figure 8. Capacitor voltage and current for 12 V DC input

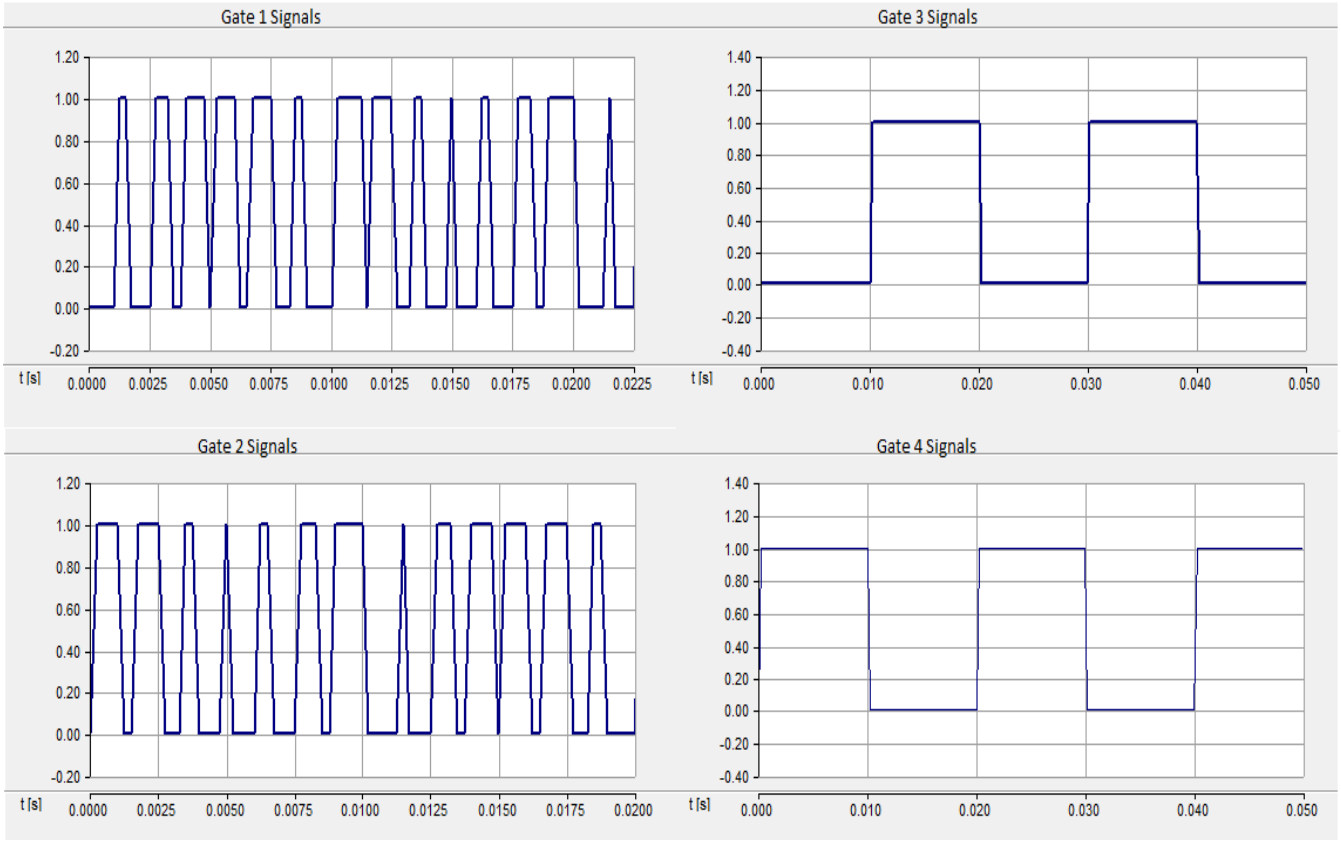


Figure 9. DC-AC Converter gate pulses

Table 3. Simulations results

| DC-DC CONVERTER | | | | | | |
|---|---|---|---|---|---|---|
| Input Voltage, $V_s$ | 12 V DC | | 24 V DC | | 36 V DC | |
| Output voltage, $V_0$ | 238.27 V DC | | 476.54 V DC | | 714.80 V DC | |
| Output current, $i_0$ | 0.238 A | | 0.476 A | | 0.714 A | |
| $L_1$ current, $i_{L1}$ | 2.31 A | 2.45 A | 4.58 A | 4.90 A | 6.88 A | 7.36 A |
| $L_2$ current, $i_{L2}$ | 2.30 A | 2.46 A | 4.56 A | 4.88 A | 6.89 A | 7.36 A |
| $L_1$ voltage, $V_{L1}$ | -47.66 V | 11.92 V | -95.35 V | 23.83 V | -142.99 V | 35.77 V |
| $L_2$ voltage, $V_{L2}$ | -47.66 V | 11.92 V | -95.31 V | 23.84 V | -143.01 V | 35.75 V |
| $C_1$ voltage, $V_{c1}$ | 11.81 V | 11.87 V | 23.68 V | 23.79 V | 35.54 V | 35.69 V |
| $C_2$ voltage, $V_{c2}$ | 119.08 V | | 238.17 V | | 353.31 V | |
| $C_3$ voltage, $V_{c3}$ | 119.16 V | | 238.27 V | | 357.42 V | |
| Switch current, $i_{sw}$ | 0 A | 9.09 A | 0 A | 14.64 A | 0 A | 22.16 A |
| Switch voltage, $V_{sw}$ | 119.04 V | 0.15 V | 238.32 V | 0.12 V | 357.56 V | 0.16 V |
| DC-AC CONVERTER | | | | | | |
| Carreier frequency, $f_c$ | 700 Hz | | | | | |
| Peak harmonic factors (out of 63) | 13th | 0.50457 | | | | |
| | 15th | 0.51256 | | | | |
| Input voltage, $V_{in}$ | 240 V DC | | | | | |
| Peak output voltage, $V_0$ | 239.27 V AC | | | | | |
| Peak output current, $i_0$ | 48 A AC | | | | | |
| Frequency, $f_0$ | 50 Hz | | | | | |

Table 4. Comparison of other SLCN DC-DC converters with the DC-DC converter in the proposed topology

| Topology | Gain | Gain at 80% duty cycle | Voltage stress across switch | $L$ | $C$ | $D$ | $S$ | Total |
|---|---|---|---|---|---|---|---|---|
| [7] | $\frac{2(1+2D)}{1-D}$ | 26 | $\frac{V_0}{2}$ | 3 | 3 | 9 | 1 | 16 |
| Proposed [10] | $\frac{4}{1-D}$ | 20 | $\frac{V_0}{2}$ | 2 | 4 | 5 | 1 | 12 |
| [1] | $D+(1+D)\frac{1+3D}{1-D}$ | 31.4 | - | 5 | 3 | 9 | 1 | 18 |
| [2] | $\frac{3+D}{1-D}D$ | 15.2 | $\frac{1+D}{1-D}V_{in}$ | 3 | 3 | 5 | 1 | 12 |

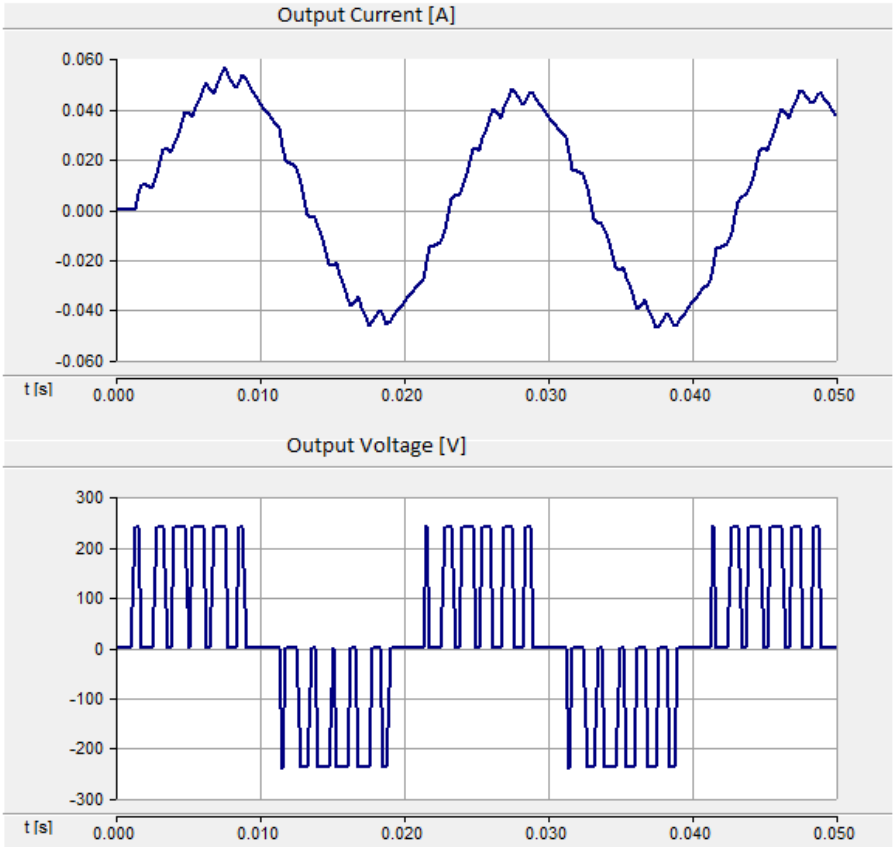


Figure 10. DC-AC converter output current and voltage waveforms

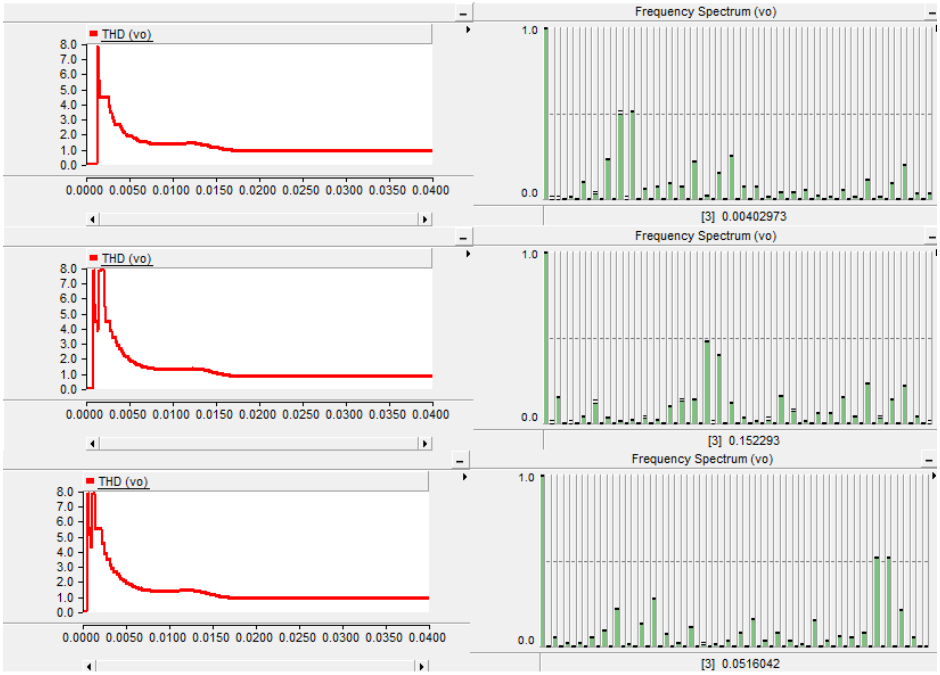


Figure 11. THD and frequency spectrums

Simulation for the DC-DC section of the proposed two stage converter was carried out with three different input voltages. The 12 V, 24 V and 36 V input voltages were used to determine the suitable of the proposed converter for varying input voltages. The respective output voltages were all boosted by a factor of 20. The output voltage magnitudes are shown in Table 3. The Figures 5 to 10 shows simulation waveforms of the proposed converter.

The only switch in the DC-DC section of the converter generated the waveform of Figure 5 i.e., the gate signal, switch current and voltage waveforms. Figure 6 shows the current and voltage waveforms of inductors $L_1$ and $L_2$. Comparing Figure 6- 4 shows the similarity between the theoretical waveform and simulation waveform. Figure 7 shows the load current and voltage for 12V input voltage. Capacitors $C_2$ and $C_3$ voltage and current waveforms are shown by Figure 8. Figure 9 shows the gate signals of the four switches for the inverter side of the converter. The AC voltage and current waveforms are shown by Figure 10. The THD and frequency spectrum of the inverter section is shown by Figure 11.

## 4. CONCLUSIONS

A two stage DC-AC converter topology with the following features; non-isolated, has a voltage gain of 20, and has reduced components, suitable for grid solar PV application is proposed in this paper. The first stage of the proposed converter is a SLCN based DC-DC converter while the second stage is an H-bridge inverter. The SLCN DC-DC converter was implemented with three different input voltages; the corresponding output voltages were all boosted by a boost factor of 20 using 80% duty cycle and 20 kHz switching frequency. Sinusoidal PWM control technique is used to control the H-bridge inverter.

Theoretical analysis of the proposed converter is provided together with simulations. PSCAD v4.2 software is used to provide output waveforms of currents and voltages of selected components. The generated output waveforms validate theoretical findings provided. The DC-DC stage provides high voltage gain for all three simulations using different input voltages; 12 V, 24 V, and 36 V, the respective output voltages are 238 V, 476 V, and 714 V. Simulations were carried out on the inverter side using 240 V DC as input and an output peak voltage of 239 V AC at 50 Hz was generated. Therefore, the proposed topology is suitable for interfacing a low DC voltage source with a high voltage DC or AC load.

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