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DSTATCOM BASED ADDITIVE AND SUBTRACTIVE TOPOLOGY MULTILEVEL INVERTER FOR IMPROVING POWER QUALITY

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Abstract- This research proposes a DSTATCOM-based innovative multilevel inverter that uses additive and subtractive topologies to achieve larger output levels. In comparison to previous topologies, this strategy the active switches are dramatically decreased. The current multilevel inverter can only generate five voltage levels. The multilevel inverter can be converted to a nine-level inverter using the proposed architecture. Furthermore, the new multilevel inverter can employ a modified hybrid multicarrier Pulse Width Modulation (PWM) approach to provide continuous switch utilization and lower THD. An appropriate modulation technique is proposed, and the proposed concept is tested with simulation studies and a hardware model. The results show that the proposed DSTATCOM based multilevel inverter has successfully improved the power quality.

Keywords: DSTATCOM, THD Reduction, PWM Scheme, Multicarrier PWM Scheme, Additive and Subtractive Topologies.

1. INTRODUCTION

Multi-stage voltage source inverters have become feasible solutions for conversion of high-power DC-AC applications over the last few decades [1]. A multi-level inverter (MLI) is a power semiconductor device with a multi-input dc level (obtained from a battery source or capacitor) and an interlocking structure that synthesizes a step waveform [2]. When compared to traditional inverters, the voltage strains the power switches have gone through in MLIs are more affordable. Furthermore, when compared to a two-level waveform generated by traditional inverters, the multilayer the harmonic profile of the waveform is improved. Other benefits of MLIs include lower dv/dt load stress ability to operate fault-tolerantly [3]. Researchers are also looking on ways to use MLIs in application with low power consumption [4].

Converter types include Neutral Point Clamped (NPC), Cascaded H-Bridge (CHB), and Flying Capacitor (FC)has all been extensively investigated and is commercially available for multilevel voltage output. However, increasing the number of output levels leads to an increase in active switches operating at the same time [5-6], increasing the system's overall cost. As a result, researchers are continuing to work on lowering the number of components in multilevel topologies using a variety of methods [7-8]. Topological changes, for example, are one of three sorts of techniques. Asymmetric sources, topological alterations, and asymmetric source configurations available for multilevel voltage output, converters have all been extensively explored and are commercially available [9-10].

The switched DC source topology, on the other hand, has a number of disadvantages [11]. As a result, we suggest a novel topology known as "Additive and Subtractive" to overcome these issues. It Principles of operation the topology is made up of 9-level single-phase inverters. A multi-carrier signal control approach is provided, along with simulation results [12]. Lastly the possible modifications that can be implemented to this newly developed MLI is addressed [13].

The output voltage waveform has a low Total Harmonic Distortion (THD) due to lower voltage stress across power switches; multilayer inverters have recently gained favors [14]. Multilevel converters have a high output power capability, Lower output harmonics and commutation losses are also advantages [15]. Their main disadvantage is their complexity, which needs a significant number of power devices and passive components, as well as complicated control circuitry. This paper establishes a novel MLI with additive and subtractive design for reduction in components counts.

This also contributes to lower manufacturing costs. The primary goal of this project is to create a single-phase, nine-level MLI with fewer components. The harmonic components level is reduced using this architecture. In comparison to traditional inverters, it requires less switches, gate drivers, and carrier signals. THD and switching stresses will be reduced using this topology and modulation approaches. For "2*n*+1" levels, standard cascaded MLI requires "*n*" number of DC sources.

In actuality, four H-bridges must be cascaded for a total of nine-level. This project presents a novel nine-level output multilevel inverter with additive and subtractive topology, as well as a comparison of the proposed and current MLIs.

2. DESIGN OF DSTATCOM BASED MULTILEVEL

A D-STATCOM is a distributed static compensation device that converts a single DC voltage to three-phase ac outputs using a two-level voltage source converter (VSC). It consists of a coupling transformer and a storage device. As illustrated in Figure 1 [7]. The VSC is linked in parallel with the ac system. It has three primary functions: 1. Reactive power compensation and voltage regulation; 2. Power factor correction; 3. Harmonics in the current are removed.

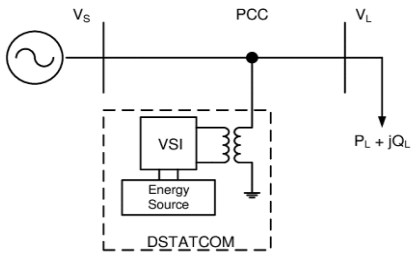

Figure 1. Schematic diagram of a DSTATCOM

2.1. ADDITIVE AND SUBTRACTIVE TOPOLOGY MULTILEVEL INVERTER

MLI is becoming more common today because of high frequency and low level THD. However, as the level rises, so must the equipment. As a result, we present the subtraction topology, a novel architecture that we combine to build very high output voltage waveforms with the fewest components. With this structure, we can generate '*n*' number of combinations.

2.1.1. Using Single DC Source

If a single DC source of voltage E1 is present, there are three possible permutations: $+E_1$, 0, and $-E_1$. When the zero level is removed, the resulting inverter can be numerous levels. Figure 2 depicts such a construction [14]. It's a single-phase full bridge inverter in the typical sense.

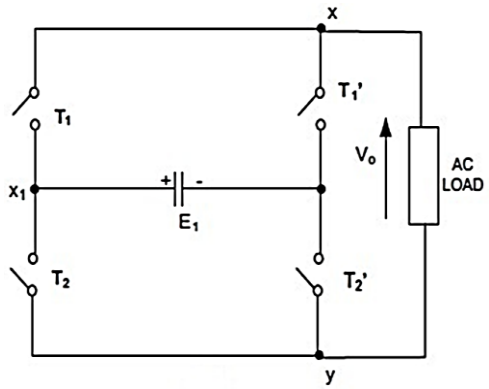

Figure 2. Inverter configuration a single DC source

2.1.2. Using Two DC Power Sources

It can be operated with a single DC source operating mode or two source combined operating mode. As a result, with two DC sources, the output waveform can be generated in nine different ways, yielding a nine-level inverter. Figure 3, depicts one such structure [13].

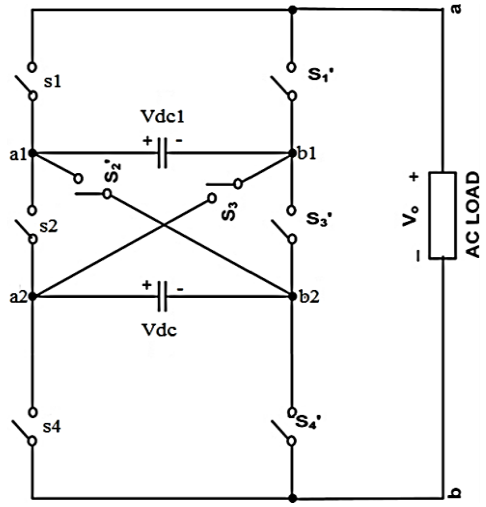

Figure 3. Layout of an inverter with two DC input sources

2.1.3. Using Three Battery Power Sources

Given 3 DC supply with voltages E_1, E_2, and E_3, the following combinations are possible:

I. Concentrate on one level at a time.
II. Operation on two level at an instant.
III. Level 3 operation at once.
IV. Zero Level due to additive and subtractive combinations leads to 27-level inverter.

2.1.4. With '*n*' different DC sources

As shown in Figure 4, the potential combinations of '*n*' different sources are used for the construction of proposed inverter.

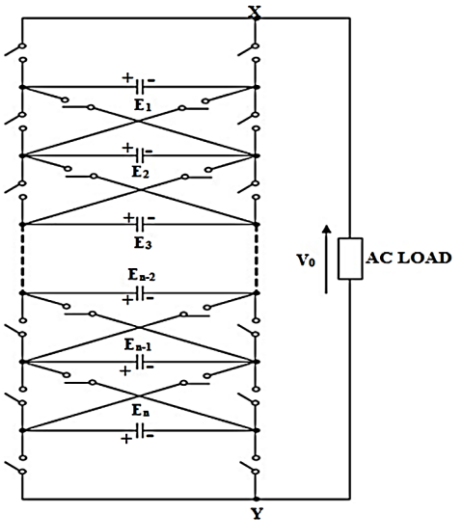

Figure 4. Single-phase proposed converter structure

3. PRINCIPLE

To demonstrate the working concept of the proposed topology, a single-phase 9-level inverter is used. It is made up of two input asymmetric DC sources, E_1 and E_2, as shown in Figure 4, with E_2 equaling E_1. For the DC source array, $E_1/E_2 = 3$ is chosen for the battery source array. As a result, this design can produce nine different output voltage values. There are numerous ways to organize DC sources in Equations (1), (2) and (3) [13].

I. If all DC sources are the same, a "unary" array is created. That is,

$$E_1 = E_2 = E_3 = ... = E_n \quad (1)$$

II. The "binary" array has a geometric progression with the DC source as an argument of "1/2". Occurs when. That is,

$$\frac{E_1}{E_2} = \frac{E_2}{E_3} = ... = \frac{E_{n1}}{E_n} = 2 \quad (2)$$

III. If the DC source geometrically advances to a coefficient of "1/3", then "A triple" array is created.

$$\frac{E_1}{E_2} = \frac{E_2}{E_3} = ... = 3 \quad (3)$$

The two sources in this topology are E_2 and E_1, with the real output being the sequence (unary, binary, or ternary). Determine how many levels there are. For example, there are five output levels when two sources E_1 and E_2 have the same value ($E_1 = E_2 = E_0$) (i.e., $\pm E_0$, $\pm 2E_0$, and 0) are available (that is, a 5-level waveform in the E_0 stage). The binary source settings ($E_1 = 2E_0$ and $E_2 = E_0$) can be used to combine seven output levels (i.e., $\pm E_0$, $\pm 2E_0$, $\pm 3E_0$, and 0). (That is, 7 levels in the E_0 stage). Waveform). A ternary source configuration ($E_1 = 3E_0$ and $E_2 = E_0$) synthesizes voltage levels ($\pm E_0$, $\pm 2E_0$, $\pm 3E_0$, $\pm 4E_0$, and 0), a 9-level waveform with E_0 steps, in a similar way.

3.1. Operation

In practice, self-commutating power switches such as MOSFETs and IGBTs can be used to implement in existing inverters. The topology contains eight switches, and three switches must be ON at the same time to achieve any specified voltage level, as shown in Figure 5 [13].

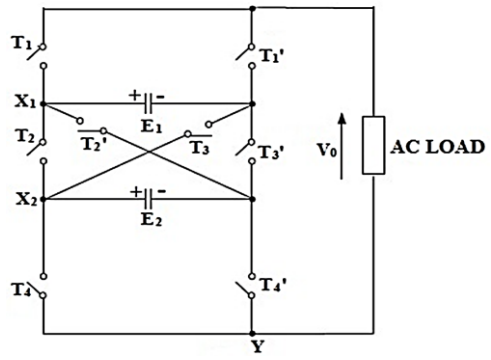

Figure 5. Proposed nine-level inverters in single phase

There are four complementary switch pairs. It's also worth noting that the switches at T_2 and T_3' must be "completely directional switches", or else undesired switching will occur.

When switches T_4', T_3', and T_1 are activated and combined voltage level is required, the anti-parallel diode of switch T_3' receives a forward voltage drop of E_2.

As a result, it functions as an ON switch, E_2 is short circuited. The switching operations occurs as discussed in the earlier case.

3.2. Modes of Operation

3.2.1. Mode 1

Mode 1 operation is used to get output voltage $V_0 = E_1$, where E_1 is the second voltage level of the nine-level inverter. In order to obtain this output voltage, the switches T_1, T_3', and T_4' conducts. Figure 6 depicts the current flow in mode-1 operation. The path of the current flow is such that E_1-T_1-LOAD-T_4'-T_3'-–E_1.

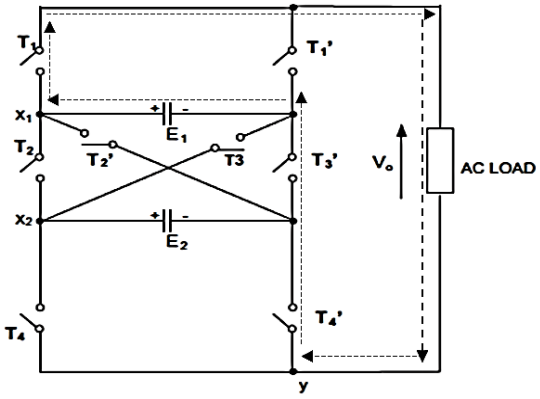

Figure 6. Current path in mode 1 operation

3.2.2. Mode 2

The output voltage $V_0 = E_2$ is obtained using Mode 2 operation. where E_2 is the 4th voltage level of the nine-level inverter. In order to obtain this output voltage, the switches T_1', T_3, and T_4' conducts. Figure 7 depicts the current flow in mode-2 operation. The path of the current flow is such that E_2-T_3-T_1'-LOAD-T_4'-–E_2.

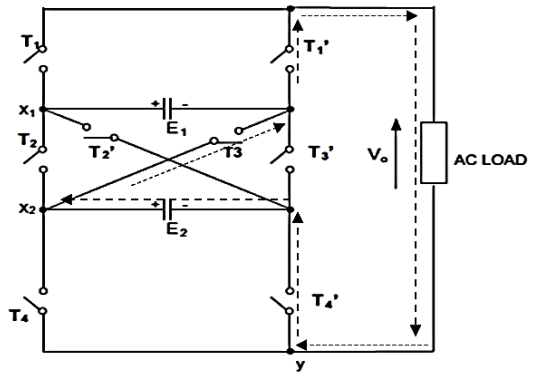

Figure 7. Current direction in Mode 2 Operation

3.2.3. Mode 3

Mode 3 operation is used to receive output voltage, $V_0 = E_1 – E_2$, where, $E_1 – E_2$ is the 3rd voltage level of the inverter. In order to obtain this output voltage, the switches T_1, T_3', and T_4 conducts. Figure 8 depicts the current flow in mode-3 operation. The path of the current flow is such that E_1-T_1-LOAD-T_4-E_2 -–E_2-T_3'-–E_1.

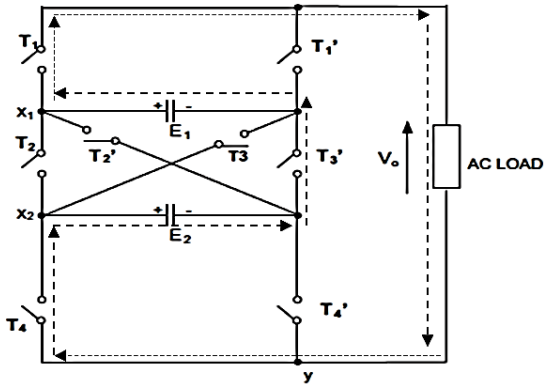

Figure 8. current flow in mode 3 operation

3.2.4. Mode 4

Mode 4 operation is used to attain output voltage $V_0 = E_1+E_2$, where E_1+E_2 is the first voltage level of the inverter. In order to obtain this output voltage, the switches T_1, T_3, and T_4' conducts. Figure 9 depicts the current flow in mode-4 operation. The path of the current flow is such that E_1-T_1-LOAD-T_4'-–E_2-+E_2-T_3-–E_1.

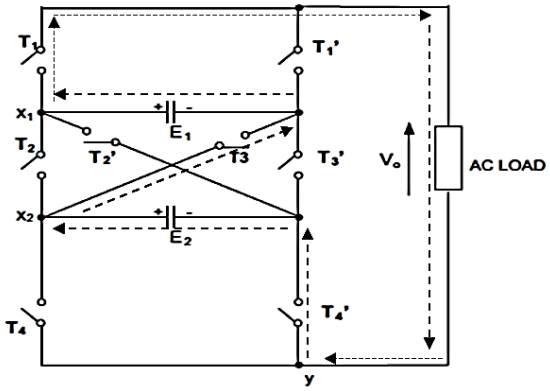

Figure 9. current way in mode 4 operation

3.2.5. Mode 5

Mode 5 operation is used to evaluate output voltage $V_0 = 0$, where 0 is the 5th voltage level of the inverter. In order to obtain this output voltage, the switches T_1', T_3', and T_4' conducts. Figure 10 depicts the current flow in mode-5 operation. The path of the current flow is such that T_1'-LOAD-T_4'-T_3'-T_1'.

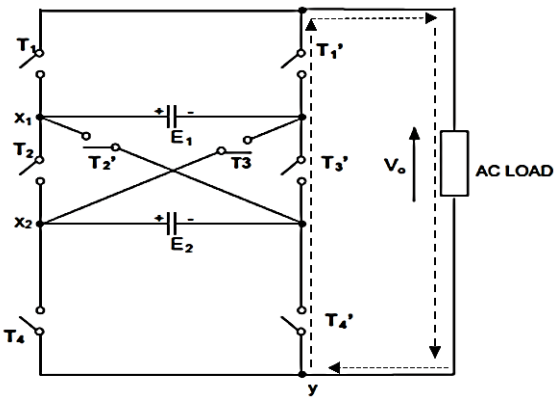

Figure 10. Current flow direction in mode 5 operation

3.2.6. Mode 6

Mode 6 operation is used to get output voltage $V_0 = –E_1$, where, $–E_1$ is the 8th voltage level of the inverter. In order to obtain this output voltage, the switches T_2, T_4, and T_1' conducts. Figure 11 depicts the current flow in mode-6 operation. The path of the current flow is such that E_1-T_2-T_4-LOAD-T_1'-–E_1.

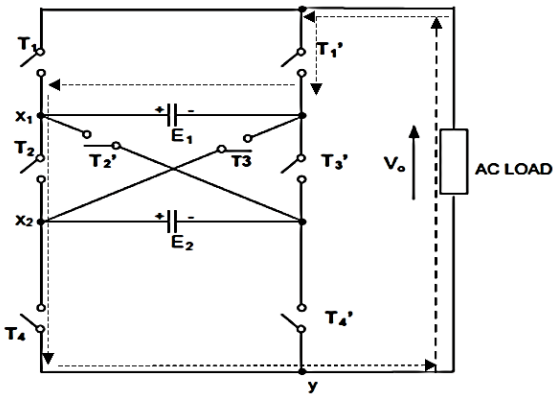

Figure 11. mode 6 current path operation

3.2.7. Mode 7

Mode-7 operation is used to obtain output voltage $V_0 = –E_2$, where, $–E_2$ is the sixth voltage level of the inverter. In order to obtain this output voltage, the switches T_1', T_3, and T_4 conducts. Figure 12 depicts the current flow in mode-7 operation. The path of the current flow is such that E_2-T_4-LOAD-T_1'-T_3'-–E_2.

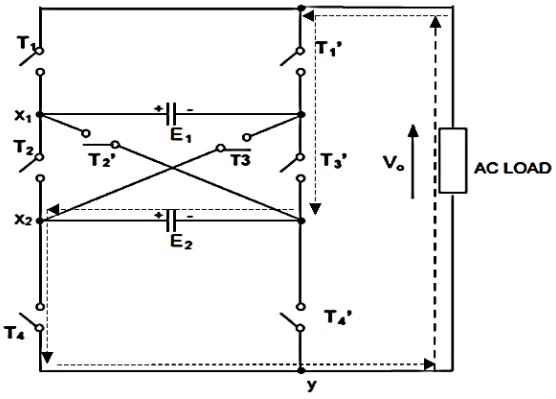

Figure 12. current way in mode 7 operation

3.2.8. Mode 8

Mode 8 operation is used to receive output voltage $V_0 = E_2–E_1$, where $E_2–E_1$ is the seventh voltage level of the inverter. In order to obtain this output voltage, the switches T_1', T_2, and T_4' conducts. Figure 13 depicts the current flow in mode-8 operation. The path of the current flow is such that E_2-T_2-E_1-–E_1-T_1'-LOAD-T_4'-–E_2.

3.2.9. Mode 9

Mode 9 operation is used to obtain output voltage $V_0 = –E_1–E_2$, where $–E_1–E_2$ is the 9th voltage level of the inverter. In order to obtain this output voltage, the switches T_1', T_2, and T_4' conducts. Figure 14 depicts the current flow in mode-9 operation. The path of the current flow is such that $–E_1$-T_1'-LOAD-T_4-E_2-–E_2-T_2'-+E_1.

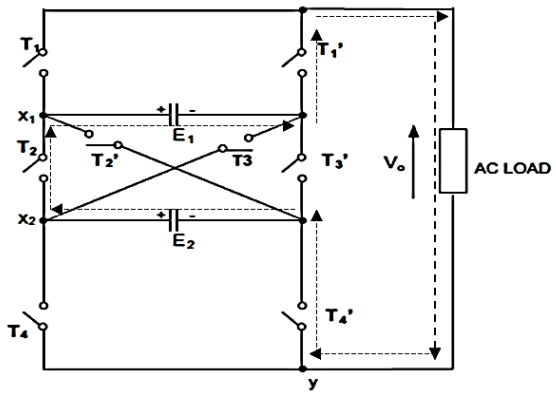

Figure 13. current flow in mode 8 operation

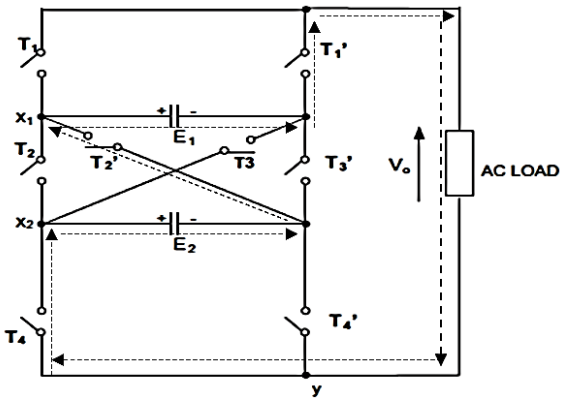

Figure 14. Current direction in mode 9 operation

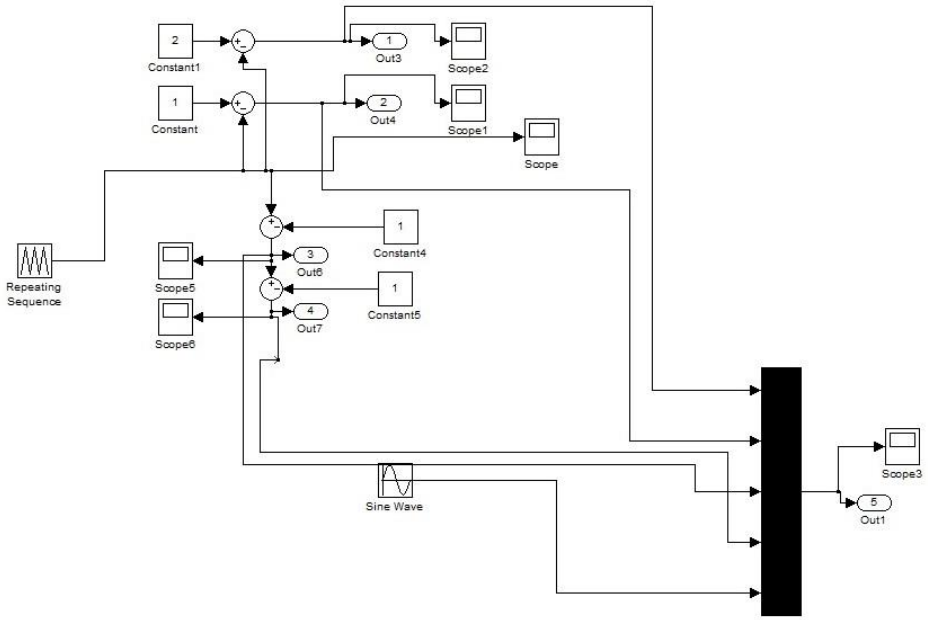

Figure 15. One phase five-level inverter overall model

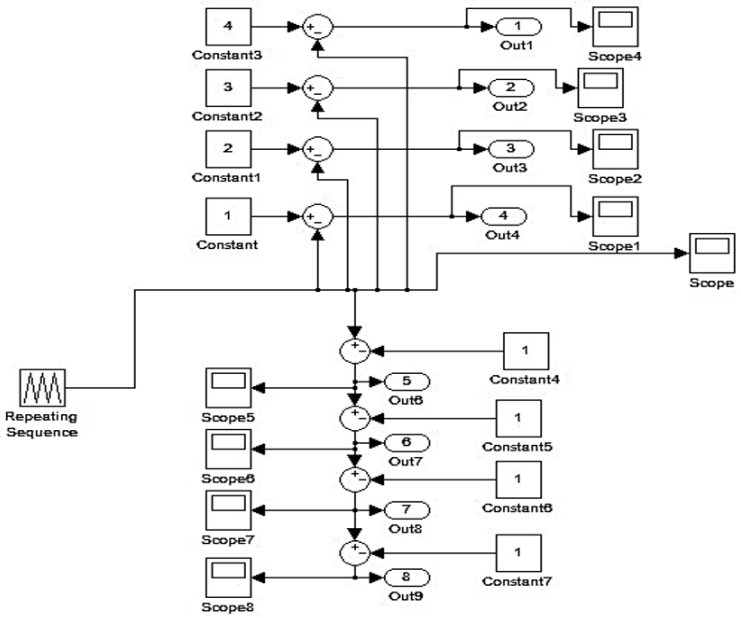

Figure 16. simulation model of pulse generation for the proposed nine-level inverter

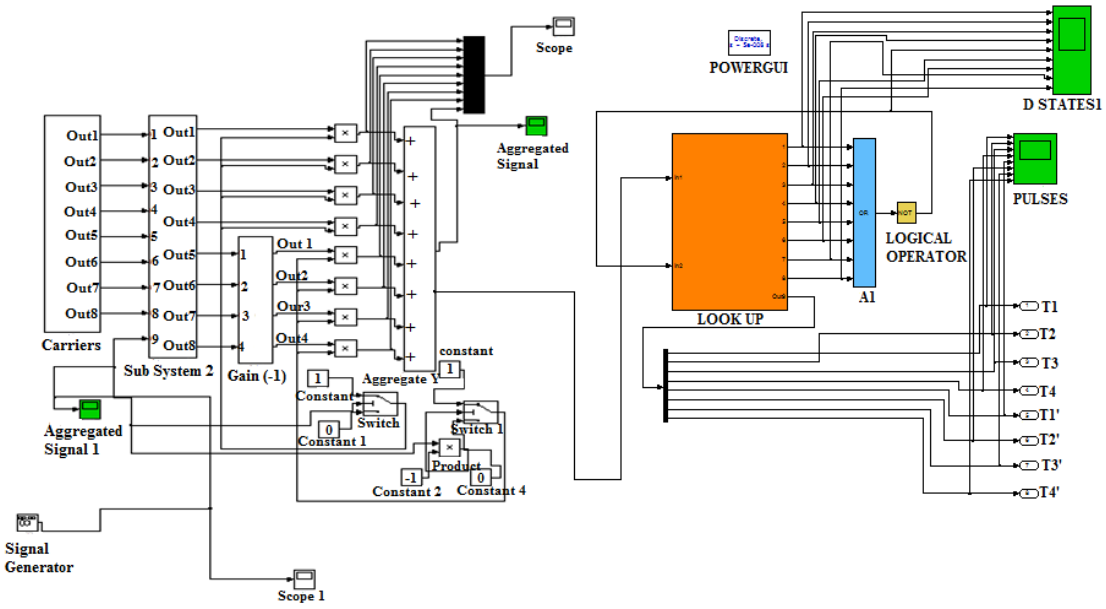

Figure 17. model of D-State generation for the proposed nine-level inverter

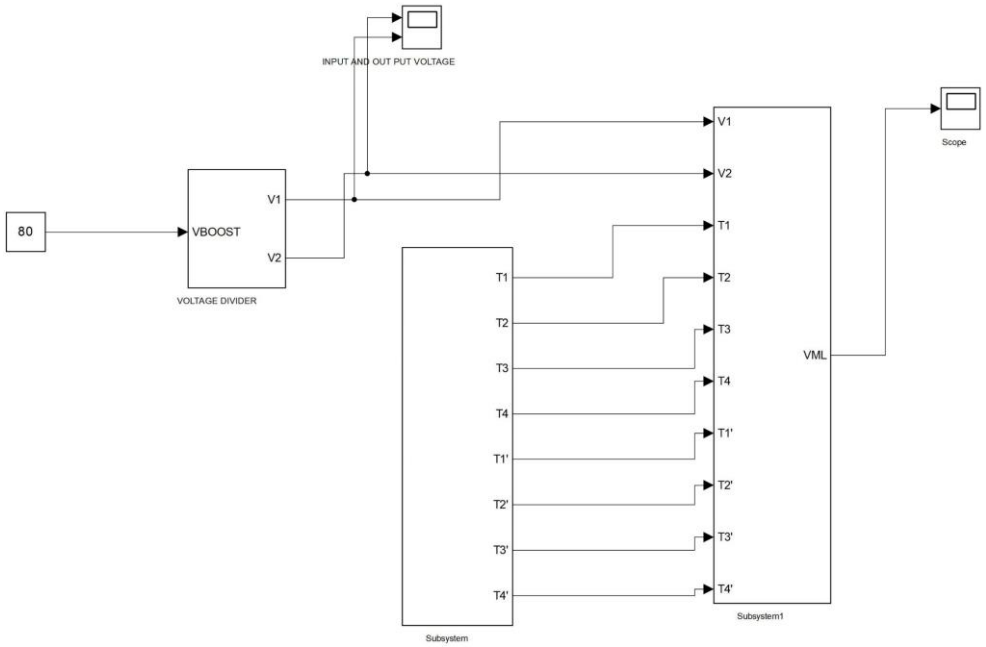

Figure 18. Simulation model of modified nine-level inverter

4. EXPERIMENTAL ANALYSIS AND SIMULATION

To investigate the performance of this existing architecture and control system, a five-level simulation system was developed. Two DC input sources are employed, such as $E_1 = E_2 = 100$ V. The modulation control circuit, pulse generator, and power circuit are all included in this simulation model. By simulating the model, a voltage of ±200 V is generated. The total simulation model for the five-level inverter is depicted in Figure 15.

4.1. Switched Nine-Level Inverter Topology

A low switching frequency multi-carrier system represents control over the proposed structure's control. In a switching device, the multi-carrier PWM method compares the carrier signal to a reference signal, and the resulting pulse corresponds to each voltage level. The numerous switches in the proposed structure, however, do not work independently of one another. As a result, unlike a two-level inverter, a proper modulation is needed to do switching. Figure 16 depicts the modulation control method.

The aggregated signal "As" is composed of signals obtained by comparing carriers to the reference sine wave. The aggregated signal "As" should resemble the output waveform. C_1, C_2, C_3, and C_4 are above the time axis carrier waveforms, whereas C_5, C_6, C_7, and C_8 are below the time axis carrier waveforms. The D-State signals are Ds1-Ds8. They are used to generate various output voltage values from 0 to (E_1+E_2). Figure 17 depicts a D-State creation simulation model [13].

Figure 18 depicts the overall simulation model for the updated nine-level inverter as a MATLAB Simulink model. The gating signals for all the switches are provided using the multicarrier PWM approach, which comprises of a voltage divider, pulse generator, and multilayer inverter.

ATMEGA16 is used to construct the control algorithm for a nine-level inverter. The circuit's hardware implementation is described. The circuit's switching device is the IRFP250N. The circuit parameters were chosen to meet the circuit's needs. The alternating current voltage, which is normally 230 V rms, the voltage level is lowered with the help of a transformer. A diode bridge rectifier is utilized to produce a proper rectified output.

This output will have ripples, which is removed with the help of a voltage regulator one of the most common voltage regulator IC modules is used to provide this voltage regulation. For optical isolation and boosting, an isolator is placed between the control unit and the driving circuit. After regulation, 15 VAC is supplied to the power circuit for MOSFET switch switching. There are eight switches and two DC sources in the power circuit. Nine output voltage levels are created by properly switching these switches.

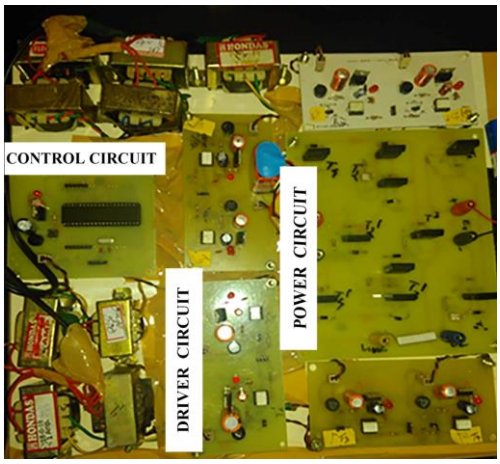

Figure 19. Hardware section

Figure 19 depicts the Hardware section of nine-level multilevel inverter consists of supply section, driver circuit, control unit with microcontroller ATMEGA16 and power circuit which is the proposed nine-level multilevel inverter, to produce a higher voltage level with reduced component count and lower THDs.

5. RESULT AND DISCUSSIONS

5.1. Switched DC Source Topology with Five Level Inverter

Figure 20 shows the output waveforms for the existing five-level inverter. The THD for the output voltage is about 27.16 percent in Figure 21 and the THD for the output current is also about 27.16 percent in Figure 22. The input voltages are E_1 = 100 V and E_2 = 100 V, respectively, for a five-level output, while the output voltage is 200 V. The aggregate signals obtained from the modulation technique are shown in Figure 23.

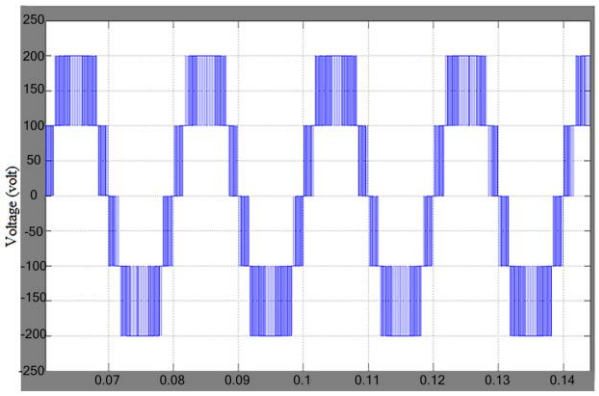

Figure 20. Five level output

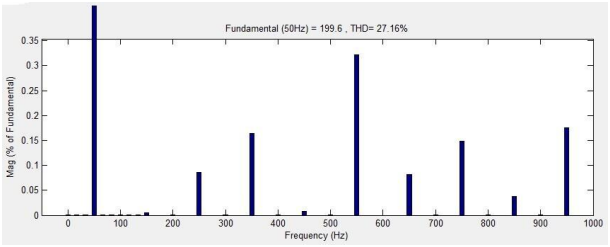

Figure 21. Five level THD output value

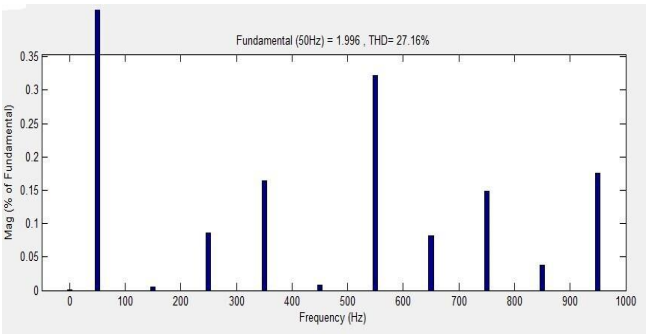

Figure 22. output current THD for five level

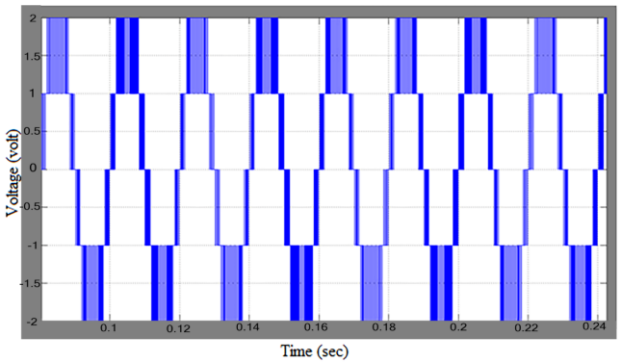

Figure 23. Aggregate signal for five level

Figure 24 shows the output waveforms for a 9-level inverter with a switched dc source configuration. The input voltage is $E_1 = E_2 = E_3 = E_4$ = 50 V, and the output voltage is 200 V to achieve nine-level at the output. The output voltage and current THDs were simulated, and a result of 23.89 percent was achieved. Figures 25 and 26 illustrate the simulated waveforms for THDs.

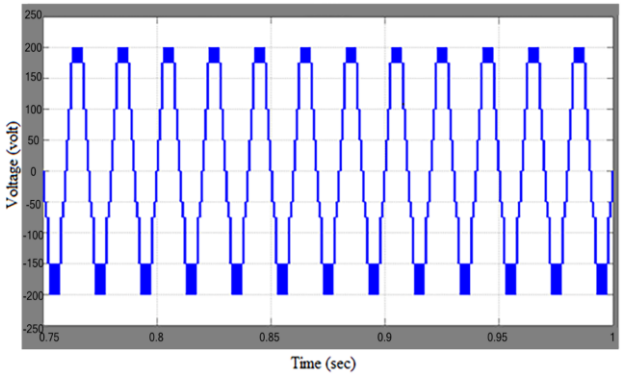

Figure 24. Existing nine-level output

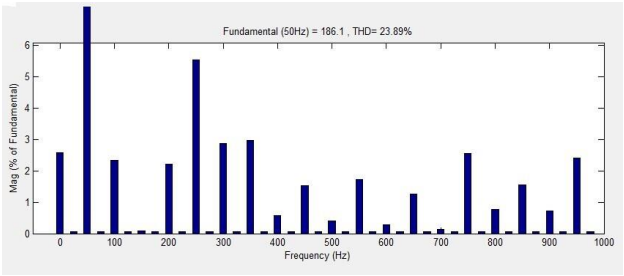

Figure 25. output voltage THD for existing nine-level

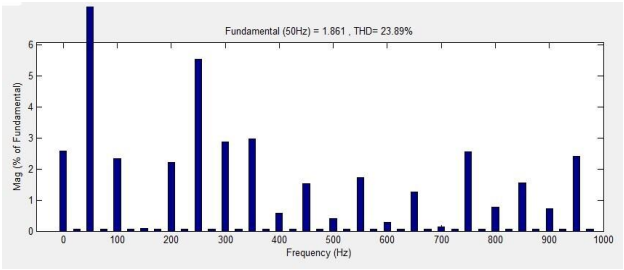

Figure 26. output current THD for existing nine-level

5.2. Nine-Level Inverter Based on Additive and Subtractive Topology

The waveform in Figure 27 depicts the output of the improved 9-level inverter.

Figures 28 and 29 show the THD values which is approximately 14.69 percent. In order to get nine-level at output, the input voltage is E_1 = 9 V, E_2 = 27 V, and the output voltage is 36 V. The D-States signals obtained from the modulation scheme are depicted in Figure 30 [13].

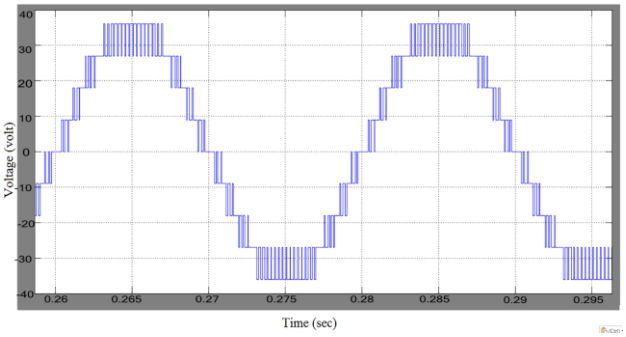

Figure 27. Proposed nine-level output

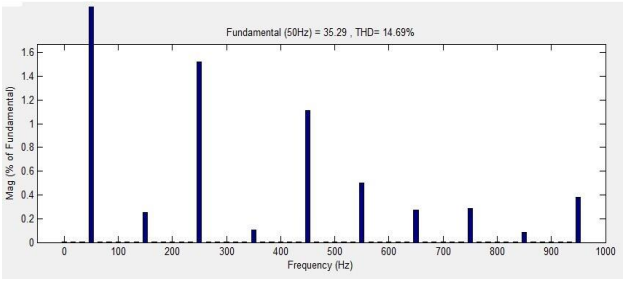

Figure 28. output voltage THD for proposed nine-level

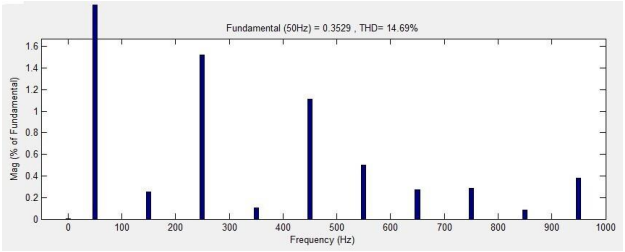

Figure 29. output current THD for proposed nine-level

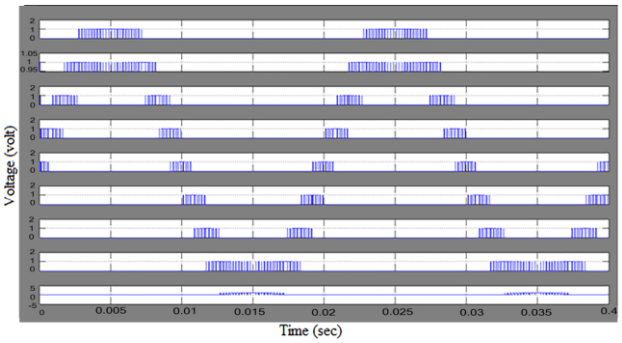

Figure 30. D-states

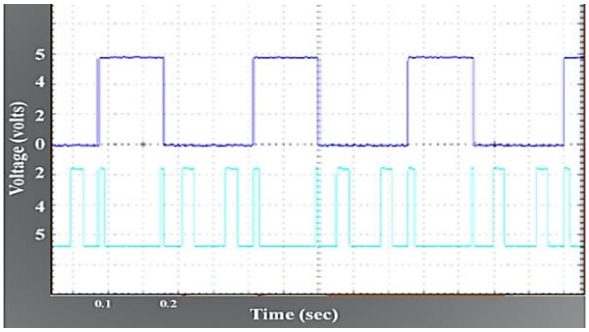

Figure 31. Generated pulses

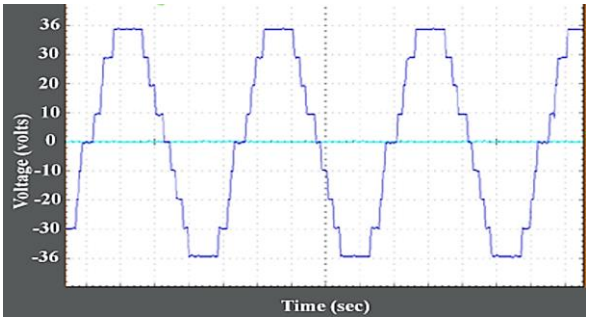

Figure 32. DSO output waveform of nine-level inverter

5.3. Comparison of Existing and Modified MLI

By comparing the output waveforms obtained by the modelled systems we can observe that the proposed system gives a higher output voltage level of nine and lower THDs of 14.69% with lower components count as compared to the existing systems. The comparison of Existing and Modified MLI is shown in Table 1 [13].

Table 1. Comparison of Existing and Modified MLI

Parameters for Comparison	Existing MLI		Modified MLI
Input source voltage	E_1=E_2=100V	E_1=E_2= E_3=E_4=50V	E_1=9V E_2=9V
Output voltage	±200V	±200V	±36V
Number of output voltage level	5	9	9
THD for output voltage	27.16%	23.89%	14.69%
THD for output current	27.16%	23.89%	14.69%
Component count	2dc Sources and 6 Switches	4dc Sources and 10 Switches	2dc Sources and 8 Switches

6. EXPERIMENTAL RESULTS

The input to the multilayer inverter circuit is a 9V, 27V battery supply. The signals from each terminal were measured using a digital storage oscilloscope, final waveforms obtained are presented below. The output waveform of the generated pulse for the switches is shown in Figure 31, and the nine-level prototype as shown in Figure 32.

Figure 33 shows the experimental arrangement with DSO for the modified nine-level MLI and thus obtained the nine-level output voltage across the load resistor. In the experimental setup it consists of power circuit, driver circuit and controller board.

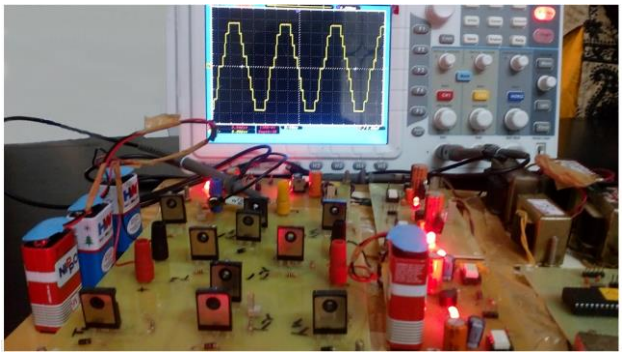

Figure 33. experimental setup with nine-level

The developed prototype produces voltage level of nine with ±36V as the output voltage for a given input of 9V and 27V. With this developed prototype it possesses lesser components count and it have lower THDs.

7. CONCLUSION

A nine-level multilevel inverter based on a modified DSTATCOM has been built, and the simulation model has been confirmed using MATLAB/Simulink. As MLI's popularity develops, attempts are being made to lower devices while maximizing output levels. This design, also known as a switched DC source topology, was created to cut down on the number of devices.

It is better to utilize a switch DC source topology control instead of a cascade inverter topology since it is less complex, less expensive, and has a lower THD percentage. This topology can only be effectively used by applications that can use an isolated DC source. Several MLI studies have been conducted in place of this, and these studies have been used to compare different topologies. Based on these studies, new DSTATCOM multi-level inverters that use addition and subtraction topologies can be developed. Implementing this topology eliminates the shortcomings of switching DC source topologies and improves stability. In addition to these multi-carrier PWM modulation techniques, uniform switches can be leveraged and applied for uniform power distribution. With the proposed topology, a hardware prototype was developed and the hardware results were obtained. Finally, we will compare the existing multi-level inverter with the modified multi-level inverter.

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