International Journal on
"Technical and Physical Problems of Engineering"
(IJTPE)
Published by International Organization of IOTPE

ISSN 2077-3528
IJTPE Journal
www.iotpe.com
ijtpe@iotpe.com

March 2023 | Issue 54 | Volume 15 | Number 1 | Pages 262-270

DYNAMIC VOLTAGE RESTORER BASED ON A NEW 31-LEVEL CASCADED INVERTER FOR POWER DISTURBANCE MITIGATIONS

S.N. Tackie

Department of Electrical and Electronic Engineering, Near East University, Nicosia, Northern Cyprus
samuel.niitackie@neu.edu.tr

Abstract- This work proposes a dynamic voltage restorer based on a 31-level single-phase cascaded inverter to mitigate power disturbances such as voltage dip and swell under various load conditions. The proposed multilevel inverter is realized by cascading two basic units coupled to an H-bridge inverter. Component count of the proposed 31-level asymmetric MLI are 12 semiconductor switches, 12 drive circuits and 4 dc sources. The proposed MLI topology boast of less component count compared to some existing topologies. Fundamental frequency modulation technique is used to control the proposed inverter because it provides reduced switching stress and reduced switching losses. The proposed DVR based MLI can offset deep or shallow and short or prolonged voltage dip and swell disturbances. Finally, the proposed DVR based MLI is built and simulated in EMTDC/PSCAD software.

Keywords: Asymmetric Multilevel Inverter, Dynamic Voltage Restorer, Fundamental Frequency Control.

1. INTRODUCTION

Power quality issues arise when the frequency, magnitude, waveform and phase of voltage along transmission or distribution lines do not match that of the source voltage. Differences in these characteristics are caused by faults at the distribution or transmission level which may lead to disturbances such as such as flickers, harmonics, unbalances voltage swell and voltage dip [1]. These disturbances if not correctly mitigated causes destruction of sensitive loads [2], disruption of production lines resulting in huge financial loss and possibly loss of vital information [3-5].

Dynamic Voltage Restorers (DVR), a member of the series compensators is regarded as the best cost-effective method of mitigating voltage disturbances. Dynamic voltage restorers are joined in series at the distribution level close to the sensitive load. Power electronic converters and injection transformers are the principal components of a DVR. Based on the converter type, dynamic voltage restorers are classified as ac-ac, dc-ac and ac-dc-ac DVRs. In ac-ac DVRs, energy storage systems are not required, compensating voltage is directly sourced from the lines and such can provide compensation for long and deep disturbances [6]. The dc-ac DVRs require energy storage systems, they are costly and have limited compensation capabilities [7]. The ac-dc-ac DVR may or may not require energy storage systems, compensating voltage is directly sourced from the lines but require double stage conversion [8].

Multilevel inverter (MLI) topologies continue to receive maximum attention because they are the preferred alternative for medium to high voltage applications. Generally, there are three conventional MLI topologies namely FC (flying capacitor), NPC (Neutral-point clamped) and CHB (cascaded H-bridge) multilevel inverters. Additionally, there are other prominent topologies such as Hybrid and Modular MLI topologies [9]. These topologies are easily controlled by any of the following PWM techniques; multi-carrier, single pulse, sinusoidal, space vector, third harmonic and fundamental frequency control [10]. Multilevel inverters offer several advantages such as such reduced *THD* content, minimum harmonic content, reduced switching losses, and minimum electromagnetic interference, reduced voltage stress on switches, utilization of lower rated switches, high efficiency, better output waveforms and suitable for medium and high-power systems [11]. Also, multilevel inverters are preferred for application in DVR, photovoltaics, electric vehicles, FACTS, electrical drives, active power filters etc. [12-13].

Various power electronic converters have been used in DVR systems for mitigation of voltage disturbances. Amongst these converters, multilevel inverters are more suitable and common since they are able to generate low, medium and high step output voltages for voltage compensations. Examples of multilevel inverter-based DVRs are; 4-level inverter-based DVR which offers better performance as against 3-level and 2-level based DVR [14]. Voltage harmonics reduction using transistor-clamped H-B inverter is presented in [15]. A cascaded multilevel inverter-based DVR having fault-current limiting capabilities is presented by [16], also, it operates in short-circuit current-limiting state and voltage unbalances and voltage fluctuation compensation state. Transformer less MLI based DVR for voltage magnitude and phase compensation was presented by [17]. In [18], a single-phase ground shifting 5-level inverter DVR having less semiconductor switches were presented.

Some DVR control techniques introduced in literature are sliding mode control [19], feedback control [20], filter-based and repetitive control [21-22], H-infinity control [23], hysteresis control [24], PLL control [22].

This work proposes a dynamic voltage restorer based on fundamental frequency controlled single-phase 31-level inverter to mitigate voltage disruptions such as voltage dip and voltage swell. The rest of this work is arranged as: proposed multilevel inverter and proposed DVR are presented in sections 2 and 3, respectively. Sections 4 and 5 describes simulation results and conclusion accordingly.

2. PROPOSED 31-LEVEL INVERTER

The basic unit of the proposed multilevel inverter is shown by Figure 1. It is made-up of 2 dc-sources and 4 unidirectional semiconductor switches. The basic topology can generate only positive output voltages i.e., it can generate 4-levels of output voltages i.e., 0 V, V_1, V_2 and V_1+V_2. The proposed cascaded topology is shown by Figure 2; it has 12 unidirectional switches and 4 dc-sources, it can generate only 15-levels of positive output voltage without an H-bridge. Therefore, H-bridge structure is required to generate negative output voltage. Hence, the proposed cascaded MLI produces 31-levels of positive and negative load voltages. Equation 1 shows the value of the source voltages in Figure 1.

$$V_1 = 1V_{dc}$$
$$V_2 = 2V_{dc} \quad (1)$$

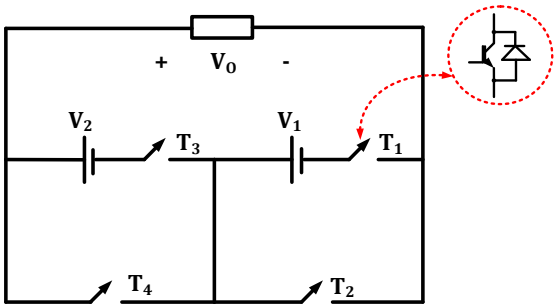

Figure 1. Basic unit of proposed multilevel inverter

The switching sequences is of the proposed cascaded multilevel inverter is shown in Table 1. In the explanation below, only positive output voltage generations are given. Switches T_9 and T_{12} are active during each of the generation sequence. Maximum voltage of $15V_{dc}$ is generated during the 15th state when switches T_1, T_3, T_5 and T_7 conducts while the remaining switches are in the voltage blocking mode. The output voltage of the 14th state is $14V_{dc}$ and in this state T_2, T_3, T_5 and T_7 are active while the remaining switches are inactive. In the 13th state, the conducting switches are T_1, T_4, T_5 and T_7, the remaining switches are non-conducting and this generates $13V_{dc}$. In the 12th state, $12V_{dc}$ is generated by conducting switches T_2, T_4, T_5 and T_7, the rest of the switches are in voltage blocking mode. During the 11th state, the active switches T_1, T_3, T_6 and T_7 generate $11V_{dc}$. In the 10th state, the conducting switches which generates $10V_{dc}$ are T_2, T_3, T_6 and T_7.

In the 9th state, active switches which produce $9V_{dc}$ are T_1, T_4, T_6 and T_7. In the 8th state, the conducting switches are T_2, T_4, T_6 and T_7 and $8V_{dc}$ is generated. During the 7th state, $7V_{dc}$ is generated by the following active switches; T_1, T_3, T_5 and T_8. In the 6th state, $6V_{dc}$ is generated by the active switches T_2, T_3, T_5 and T_8 while the remaining switches are in blocking state. During the 5th state, the active switches are T_1, T_4, T_5 and T_8 and the produced voltage is $5V_{dc}$. In the 4th state, conducting switches are T_2, T_4, T_5 and T_8 and the generated output voltage is $4V_{dc}$. During the 3rd state, the generated voltage is 3 V_{dc} by the following conducting switches T_1, T_3, T_6 and T_8. In the 2nd state, produced voltage is $2V_{dc}$ by the following conducting switches T_2, T_3, T_6 and T_8 and finally the 1st state produces V_{dc} voltage when the following switches T_1, T_4, T_6 and T_8 are active. Zero voltage can be produced by three different methods. In the first method, the following switches are turned-on T_2, T_4, T_6, T_8, T_9 and T_{10}, in the second method only switches T_9 and T_{10} active and finally in the third method, only switches T_{11} and T_{12} are active. The theoretical output waveform of the proposed cascaded MLI is illustrated by Figure 4.

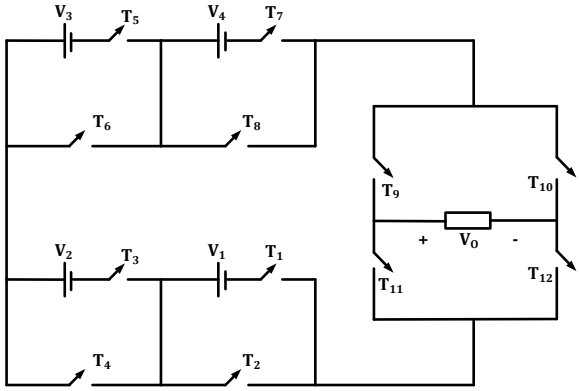

Figure 2. Proposed cascaded multilevel inverter

Table 1. Switching Pattern

State	Switches	DC Sources	Output Voltage
1	T_1, T_4, T_6, T_8	V_1	$1V_{dc}$
2	T_2, T_3, T_6, T_8	V_2	$2V_{dc}$
3	T_1, T_3, T_6, T_8	$V_1 + V_2$	$3V_{dc}$
4	T_2, T_4, T_5, T_8	V_3	$4V_{dc}$
5	T_1, T_4, T_5, T_8	$V_1 + V_3$	$5V_{dc}$
6	T_2, T_3, T_5, T_8	$V_2 + V_3$	$6V_{dc}$
7	T_1, T_3, T_5, T_8	$V_1 + V_2 + V_3$	$7V_{dc}$
8	T_2, T_4, T_6, T_7	V_4	$8V_{dc}$
9	T_1, T_4, T_6, T_7	$V_1 + V_4$	$9V_{dc}$
10	T_2, T_3, T_6, T_7	$V_2 + V_4$	$10V_{dc}$
11	T_1, T_3, T_6, T_7	$V_1 + V_2 + V_4$	$11V_{dc}$
12	T_2, T_4, T_5, T_7	$V_3 + V_4$	$12V_{dc}$
13	T_1, T_4, T_5, T_7	$V_1 + V_3 + V_4$	$13V_{dc}$
14	T_2, T_3, T_5, T_7	$V_2 + V_3 + V_4$	$14V_{dc}$
15	T_1, T_3, T_5, T_7	$V_1 + V_2 + V_3 + V_4$	$15V_{dc}$
16	T_2, T_4, T_6, T_8	-	0

The component count of the proposed cascaded 31-level inverter is determined by Equation (2) to Equation (7), where $N_{switches}$, N_{IGBT}, N_{Level}, N_{Driver} and $N_{DC\text{-}Source}$ corresponds to switch count, IGBT count, output voltage level, driver circuit count and dc source count respectively.

Note, n is the quantity of basic units employed in the cascaded architecture.

$$N_{switches} = 4n + 4 \quad (2)$$

$$N_{IGBT} = 4n + 4 \quad (3)$$

$$N_{Level} = 4n^3 - 1 \quad (4)$$

$$N_{Driver} = 4n + 4 \quad (5)$$

$$N_{DC-Source} = 2n \quad (6)$$

$$V_{o,\max} = 15V_{dc} \quad (7)$$

2.1. Fundamental Frequency Control

Nearest level control (NLC) also known as fundamental frequency control (FFC) is employed in switching the proposed single-phase multilevel inverter. Figure 3 shows the concept of NLC operations in producing 7-levels of load voltage. To generate each voltage level, the reference voltage is juxtaposed to the step output voltage, the intersecting point determines the voltage level to be selected. If this point is closer to upper voltage level, then that magnitude of output voltage is generated. However, if the point is closer to the lower voltage level, then that magnitude of voltage is generated. Basically, NLC enables selection of closest (nearest) voltage level to be generated by the proposed MLI.

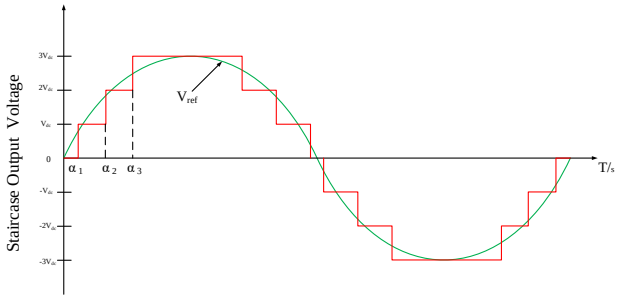

Figure 3. NLC technique

2.2. Power Losses Computation

This section provides power losses computation of the proposed MLI. This is determined by calculating the power losses during switching and conduction. Switching power losses (P_{SW}) expressed by Equation (8) occurs during the switching period of switch-on (turn-on) and switch-off (turn-off) of individual switches. The E_{on} and E_{off} represent switch-on and switch-off of inverter energy loss accordingly, f_s is the switching frequency, t_{on} and t_{off} are the switch-on time and switch-off time accordingly.

$$P_{SW} = f_s \sum_{k=1}^{N_{switch}} \left(\sum_{i-1}^{N_{on,\,k}} E_{on,k} + \sum_{i=1}^{N_{off,\,k}} E_{off,k} \right) \quad (8)$$

Conduction losses occur when the power switches are conducting. The applied semiconductor switches of the proposed MLI are unidirectional switches with respect to the voltage and each switch is composed of one diode which antiparallel connected to an IGBT. Therefore, the conduction power losses of the diode ($P_{C,D}$) and IGBT ($P_{C,T}$) are computed separately and summed-up to give the conduction power losses of the converter (P_C). The value of β is dependent on the type of semiconductor switch employed and it's a constant value provided by the manufacturer. The diode and transistor resistance are expressed by R_D and R_T accordingly. Similarly, the voltage across the diode and the transistor are expressed by V_D and V_T accordingly. Solving Equation (9) and Equation (10) will yield Equation (11).

$$P_{C,T} = \frac{1}{2\pi} \int_0^{2\pi} n_T(t)[V_T + R_T i^{\beta}(t))i(t)]d(\omega t) \quad (9)$$

$$P_{C,D} = \frac{1}{2\pi} \int_0^{2\pi} n_D(t)[(V_T + R_D i(t))i(t)]d(\omega t) \quad (10)$$

$$P_C = P_{C,T} + P_{C,D} \quad (11)$$

Therefore, absolute power loss P_{Loss} of the inverter is computed by:

$$P_{Loss} = P_{sw} + P_C \quad (12)$$

Efficiency η of the inverter computed by:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{in} - P_{Loss}}{P_{in}} \quad (13)$$

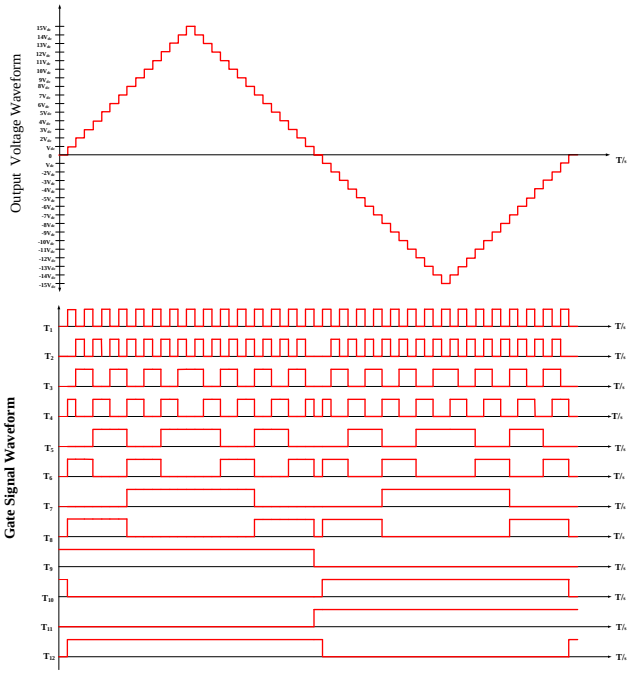

Figure 4. Theoretical output voltage and gate signal waveform of proposed inverter

3. PROPOSED CASCADED MLI BASED DVR

Figure 5 represents the circuit configuration of the proposed MLI-DVR topology. The DVR and the distribution lines are cascaded at the PPC area (point of common coupling) by the help of an injection transformer. The single-phase transformer acts as an isolator and voltage injecting device. Principle of operation of the DVR is categorized into two modes; voltage injecting mode and zero voltage injecting mode. In voltage injecting mode, disturbances such as voltage dip, flickers and voltage swell are mitigated by injecting suitable voltage with opposite phase or magnitude. During zero voltage injecting mode, no disturbances are detected and as such, the cascaded inverter generates zero voltage which is injected into the grid by activating by-pass switch S.

Four voltages exist in the proposed *DVR* topology of Figure 5. These voltages are grid voltage (V_G), load voltage (V_L), DVR voltage (V_D) and cascaded inverter output voltage (V_{IN}), $V_D = V_{IN}$. The general single-phase DVR differential equations are expressed as:

$$UV_{dc} - V_{DVR} = L_f \frac{di_F}{dt} \quad (14)$$

$$i_F - i_G = C_f \frac{dV_{DVR}}{dt} \quad (15)$$

The grid current is given by i_G , filter or inverter output current is given by i_F, V_{DVR} is the DVR injected voltage, filter capacitance, source voltage and filter inductance are given by C_f, V_{dc} and L_f accordingly. U is the source control parameter. The voltage disturbance (sag or swell) magnitude to be compensated is determined when the grid voltage (V_G) is subtracted from the reference grid voltage (V_{ref}). If the result is more or less than the reference voltage, then voltage swell or sag has occurred. Therefore, the voltage to be injected is expressed by Equation (16) and the load voltage (V_L) is given by Equation (17).

$$V_{DVR} = V_{ref} - V_G \quad (16)$$

$$V_L = V_G + V_{DVR} \quad (17)$$

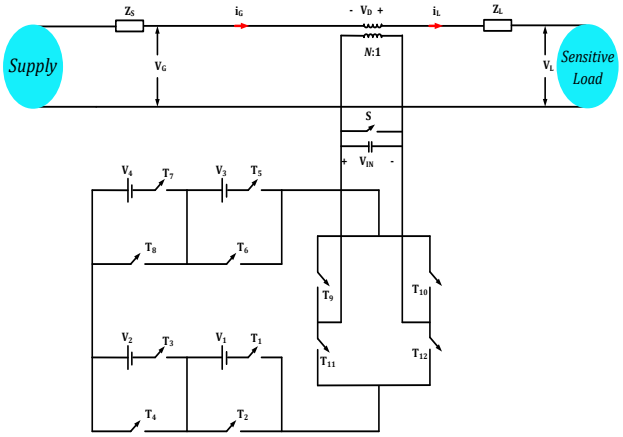

Figure 5. Proposed cascaded MLI based DVR

Based on Equation (16), the load voltage should always be at its rated value. During zero voltage injecting mode, the load voltage will be equal to the grid voltage (V_L=V_G) i.e., V_{DVR} injects zero voltage (V_{DVR}=0). However, during non-zero voltage injecting mode $V_{DVR} \neq 0$. Therefore, the cascaded inverter generates the suitable DVR voltage for compensation. During sag and swell disturbances, Voltage sag (V_{SAG}) and voltage swell (V_{SWELL}) magnitudes are computed below by:

$$V_{SAG} = V_{L,REF} - V_G \quad (18)$$

$$V_{SWELL} = V_{L,REF} - V_G \quad (19)$$

where, $V_{L,REF}$ is the nominal load voltage. During voltage sag disturbance, V_G is less than $V_{L,REF}$, therefore, V_{SAG} equals to positive voltage. Similarly, during voltage swell condition, V_G is greater than $V_{L,REF}$, therefore, V_{SWELL} equals to negative voltage.

During compensation, inverter voltage V_{DVR} generates negative and positive voltages for voltage swell and voltage sag compensation accordingly.

$$V_{DVR} = +V_{SAG} \quad (20)$$

$$V_{DVR} = -V_{SWELL} \quad (21)$$

3.1. Limitation of Proposed MLI Based DVR

This section investigates voltage compensation capabilities of the proposed dynamic voltage restorer based on a 31-level cascaded inverter. The following parameters are important for this investigation; input voltage magnitude, maximum/peak inverter output voltage, load voltage, incremental voltage levels and compensating percentage. The peak inverter output voltage and incremental voltage levels are of outermost importance because they determine the maximum magnitude of voltage the DVR can inject and the magnitude of step injecting voltage. Another major concern of DVRs is the duration of compensation they can provide. However, the duration of compensations is not a major issue for the proposed topology because several dc sources such as photovoltaic systems etc. can be used. For maximum inverter output voltage, asymmetric input voltage is preferred.

Five cases of varying voltages are presented for the analysis. These cases are shown in Table 2. Each of these cases have different voltage magnitudes and they can be categorized into symmetric or asymmetric. The input voltage of the proposed inverter is V_1, V_2, V_3 and V_4. In the 1st case, all input voltage has a magnitude of 10 V i.e., symmetrical input voltage. Therefore, the maximum inverter output voltage is 40 V.

Table 2. Limitation analysis of the proposed three-phase MLI based DVR

CASE	MLI Input Voltage	PIOV	IVL	RLV	CP
I	V_1 = 10 V V_2 = 10 V V_3 = 10 V V_4 = 10 V	40 V	10 V	240 V	16.67%
II	V_1 = 10 V V_2 = 10 V V_3 = 20 V V_4 = 20 V	60 V	10 V	240 V	25%
III	V_1 = 10 V V_2 = 20 V V_3 = 30 V V_4 = 40 V	100 V	10 V	240 V	41.67%
IV	V_1 = 10 V V_2 = 20 V V_4 = 40 V V_4 = 80 V	150 V	10 V	240 V	62.5%
V	V_1 = 15 V V_2 = 30 V V_3 = 60 V V_4 = 120 V	225 V	15 V	240 V	93.75%

NOTE: PIOV: Peak Inverter Output Voltage. IVL: Incremental Voltage Levels. RLV: Rated Load Voltage. CP: Compensating Percentage

This means that in the advent of voltage sag or swell conditions, the proposed multilevel inverter-based DVR can only compensate 16.67% of the load voltage (240 V) with 10 V incremental steps.

In the 2nd case, the first two input voltage are symmetrical and the last two input voltages are also symmetrical. However, all input voltages are described are semi-symmetrical, V_1 and V_2 = 10 V and V_3 and V_4 = 20 V. The maximum inverter output voltage is 60V. This means that in the advent of voltage sag or swell conditions, the proposed multilevel inverter-based DVR can only compensate 25% of the load voltage (240 V) with 10 V incremental steps. In the 3rd, 4th and 5th cases, all input voltage is different i.e., asymmetric input voltage. However, the 3rd and 4th cases have equal incremental voltage levels of 10 V, the incremental voltage level of the 5th case is 15 V. It is evident that by utilizing asymmetric input voltages, the compensating capabilities of the proposed DVR is significantly increased. The 3rd case provides 41.67% voltage compensation with a maximum output voltage of 100 V. The 4th and 5th cases provide 62.5% and 93.75% voltage compensation with maximum input voltages of 150 V and 225V, respectively.

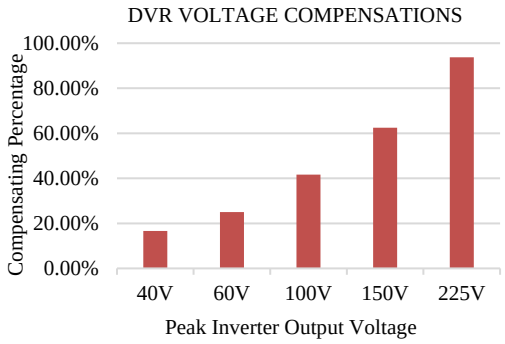

Figure 6. Compensation percentage of proposed DVR

Figure 6 shows a graph of the maximum DVR/inverter output voltage and the maximum compensating percentage. By varying the value of the source voltage, the percentage of voltage compensation is improved significantly. If the load voltage is varied while the DVR output voltages are maintained, the compensating percentage will vary. The compensating percentage will increase if the load voltage is reduced from its current value of 240 V. However, the compensating percentage will reduce if the load voltage is increased. These analyses are only valid if input voltages are maintained as in Table 2.

4. SIMULATION RESULTS

Simulation studies of the proposed dynamic voltage restorer based on a 31-level inverter is provided in this section. Analysis of the proposed inverter was done by building its power circuit in PSCAD/EMTDC software.

Table 3 depicts the simulation parameters for the proposed dynamic voltage restorer based MLI. Simulation results of the proposed dynamic voltage restorer based on 31-level multilevel inverter are illustrated below from Figure 7 to Figure 13. The waveform of the load voltage is depicted by Figure 7. The waveform of the load current is depicted by Figure 8. The peak-to-peak load voltage is 225 V with a frequency of 50 Hz. Varying the magnitude of input voltages will vary the output voltage magnitude. The load current waveform has a peak value of 4.23 A.

Table 3. Simulation Parameters

Parameters	Magnitude
DC Sources V_{dc}	$V_1 = 15$ V, $V_2 = 30$ V $V_3 = 60$ V, $V_4 = 120$ V
Modulation Index	1
Load Resistance R	50 Ω
Load Inductance L	0.055 H
Switching Frequency f_s	50 kHz
Load frequency f_o	50 Hz

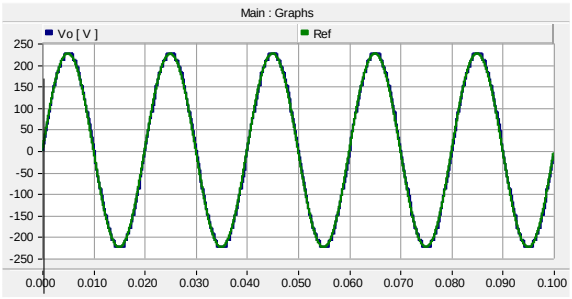

Figure 7. Load voltage and reference voltage waveforms

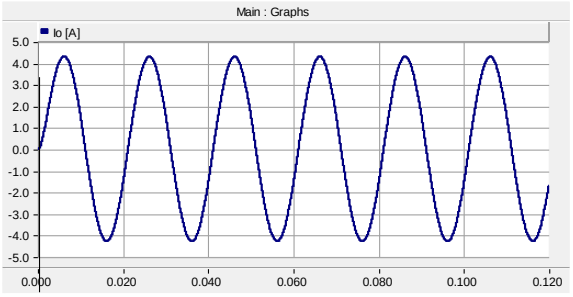

Figure 8. Load current waveform

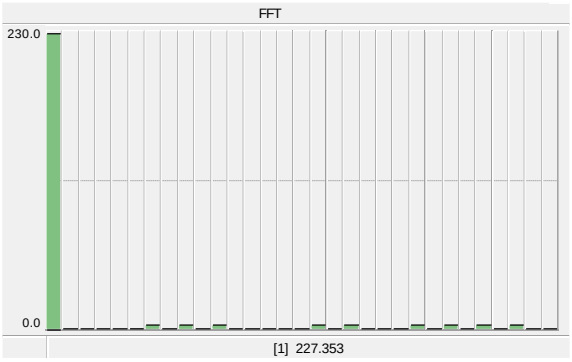

Figure 9. FFT waveform

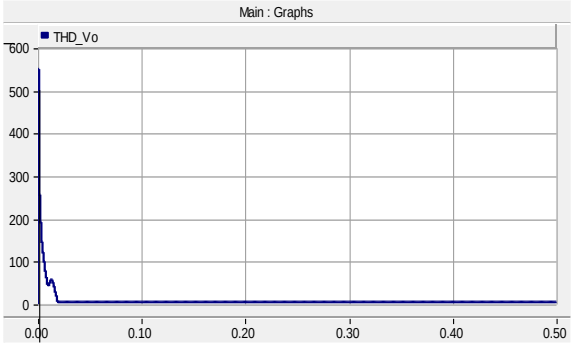

Figure 10. *THD* waveform

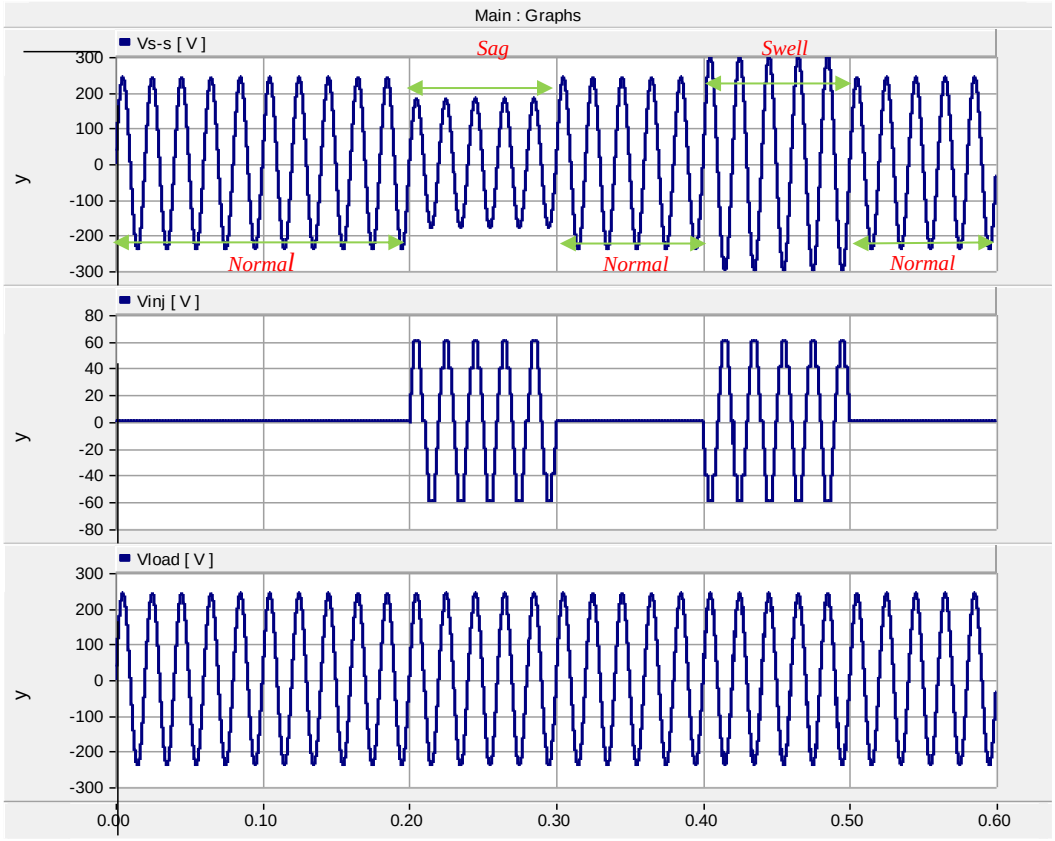

Figure 11. The 1st case of voltage sag and swell condition

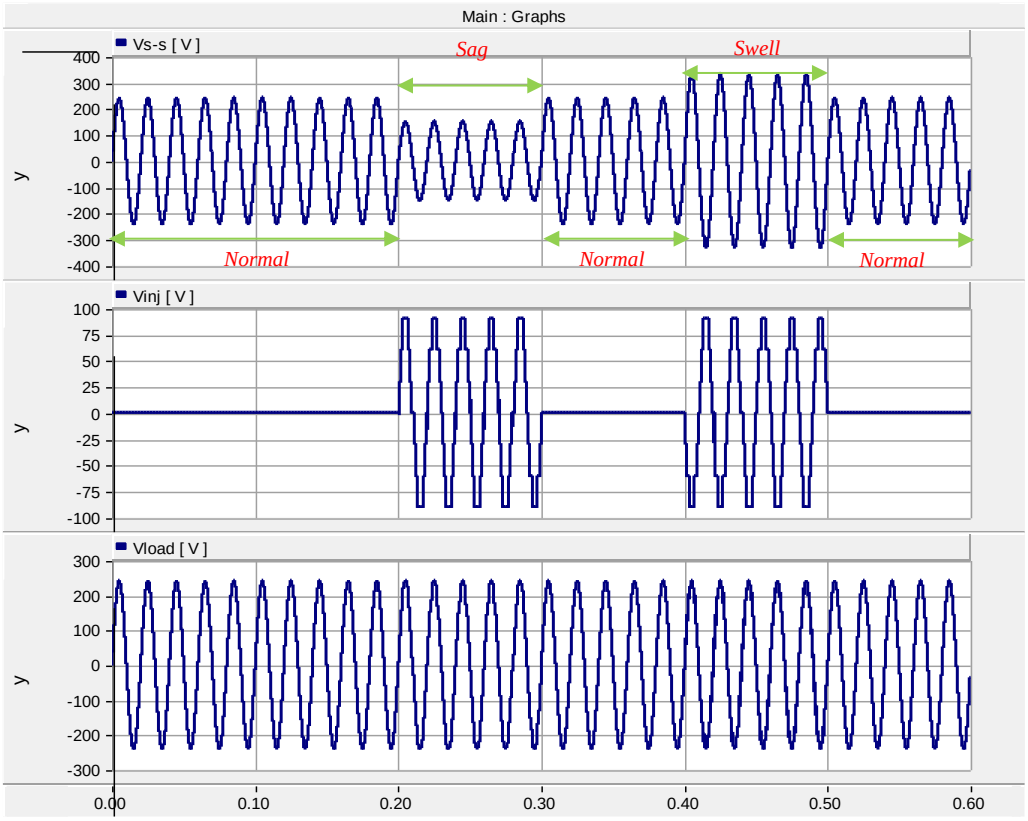

Figure 12. The 2nd case of voltage sag and swell condition

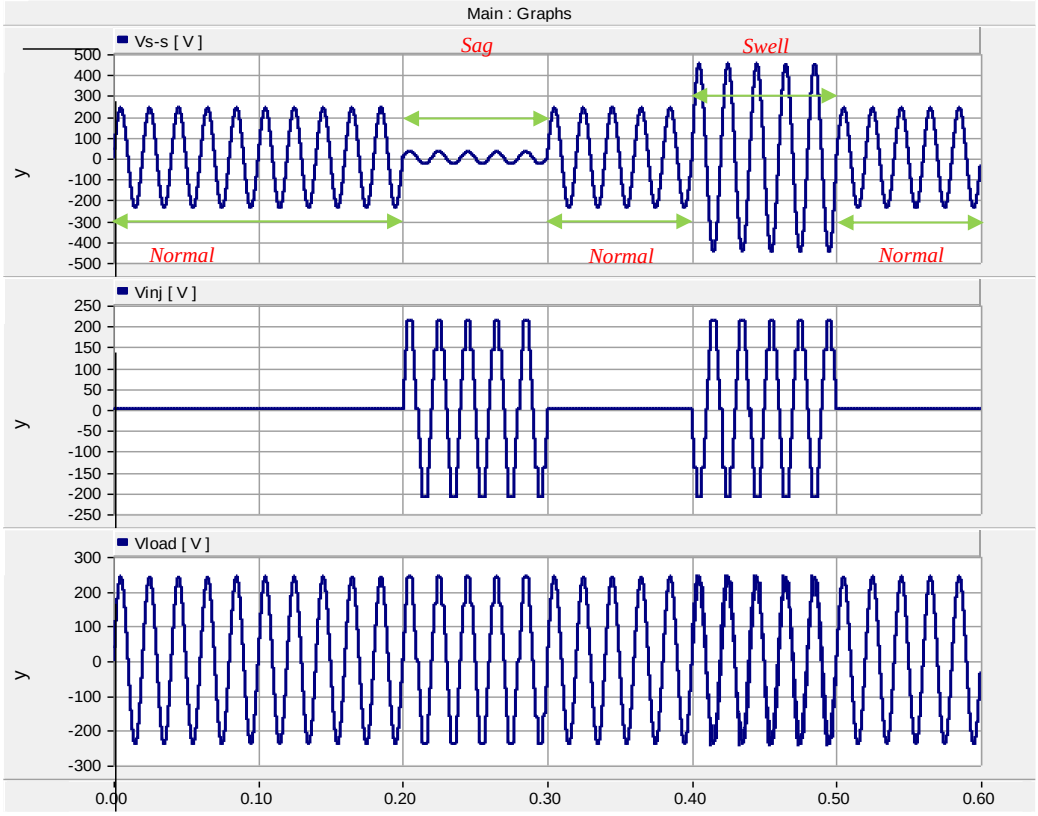

Figure 13. The 3rd case voltage sag and swell condition

Figures 9 and 10 show the FFT and *THD* waveforms of the proposed multilevel inverter. As shown in Figure 9, the magnitude of the fundamental frequency is 225 V approximately. Even order harmonics are naturally deleted i.e., equals to zero. The value of the lower order harmonics is relatively low i.e., the amplitudes of the lower order harmonics are low. For example, the 3rd and 5th harmonics have rms amplitudes of 0.597 and 0.949 respectively. Figure 10 shows the *THD* output waveform of the proposed multilevel inverter. The *THD* content of the proposed multilevel inverter is 3.082% which is less than the 5% standard percentage in power systems.

Figure 11 to Figure 13 illustrates three cases of voltage dip and swell dispositions for the proffered DVR. The period of the waveform is 0.6s. In the 1st case, represented by Figure 11, the period of normal operations (zero voltage injecting mode) is 0-0.2, 0.3-0.4 and 0.5-0.6 seconds. The period of voltage sag and voltage swell conditions are 0.2-0.3 and 0.4-0.5 seconds, respectively. The voltage sag and swell magnitudes are 180 V and 300 V accordingly. The load voltage is 240V. Therefore, the DVR injects +60 V and -60 V respectively to compensate the sag and swell conditions. In the 2nd case, represented by Figure 12, the period of normal operations is 0-0.2, 0.3-0.4 and 0.5-0.6 seconds. The period of voltage sag and voltage swell conditions are 0.2-0.3 and 0.4-0.5 seconds respectively. The voltage sag and swell magnitudes are 150 V and 330 V accordingly. The load voltage is 240 V. Therefore, the DVR injects +90 V and -90 V respectively to compensate the sag and swell conditions. Finally, in the 3rd case, represented by Figure 13, the period of normal operations is the same as the 1st and 2nd cases.

The period of voltage sag and voltage swell conditions are 0.2-0.3 and 0.4-0.5 seconds respectively. The voltage sag and swell magnitudes are 30 V and 450 V accordingly. The load voltage is 240 V. Therefore, the DVR injects +210 V and -210 V respectively to compensate the sag and swell conditions.

5. CONCLUSIONS

A new cascaded 31-level single-phase inverter based dynamic voltage restorer is proposed by this paper for voltage sag and swell mitigation. The proposed dynamic voltage restorer based on a 31-level cascaded inverter is composed of less components i.e., 12 semiconductor switches and driver circuits respectively and 4 dc sources. The major advantages of the proposed multilevel topology are high quality output waveforms i.e., the output waveforms contain less harmonics and *THD* therefore, output filter is not required, the cascaded structure is less complex and easy to control. Also, the proposed multilevel can generate higher output voltage as well as low level step output voltage. The proposed multilevel is controlled by fundamental frequency control which provides high efficiency because the switching losses are minimized.

The proposed multilevel inverter is utilized in DVR for power disturbance mitigations. Limitation investigation of the proposed DVR shows that utilizing asymmetric voltage magnitude at the inverter input enables the proposed DVR to provide voltage compensations of over 90% compared to 16.67% for symmetric voltage input. Also, asymmetric voltage input provides much higher output voltage compared to symmetric input voltage. This enables the proposed DVR to provide deeper voltage

compensation for sag and swell conditions. Finally, the proposed dynamic voltage restorer based on 31-level inverter was evaluated under three separate voltage dip and swell conditions. In all three cases, the proposed dynamic voltage restorer efficiently mitigated the voltage dip and swell conditions.

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BIOGRAPHY

Name: **Samuel**
Middle Name: **Nii**
Surname: **Tackie**
Birthday: 27.03.1988
Birth Place: Accra, Ghana
Bachelor: Electrical and Electronic Engineering, Department of Electrical and Electronic Engineering, Faculty of Engineering, Ho Technical University, Ho, Ghana, 2007
Master: Electrical and Electronic Engineering, Department of Electrical and Electronic Engineering, Engineering Faculty, Near East University, Nicosia, Northern Cyprus, 2015
Doctorate: Electrical and Electronic Engineering, Department of Electrical and Electronic Engineering, Engineering Faculty, Near East University, Nicosia, Northern Cyprus, 2021
The Last Scientific Position: Assist. Prof., Department of Electrical and Electronic Engineering, Engineering Faculty, Near East University, Nicosia, Northern Cyprus, 2021
Research Interests: Power Electronics, Renewable Energy Sources, Power Quality
Scientific Publications: 10 Papers
Scientific Memberships: IEEE